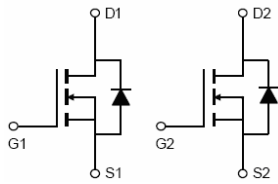


P-Channel Enhancement Mode Field Effect Transistor

DFN5X6-8L



Schematic diagram



Top View

Product Summary

- V_{DS} -30V
- I_D -18A
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) <25mohm
- $R_{DS(ON)}$ (at $V_{GS} = -10V$) <18mohm

General Description

- Trench Power MV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	-30	V
Gate-source Voltage	V_{GS}	± 10	V
Drain Current ^B	I_D	$T_A=25^\circ\text{C}$ @ Steady State	-18
		$T_A=100^\circ\text{C}$ @ Steady State	-12.6
Drain Current ^B	I_D	$T_A=25^\circ\text{C}$ @ Steady State	-18
		$T_A=70^\circ\text{C}$ @ Steady State	-12.6
Pulsed Drain Current ^A	I_{DM}	-55	A
Single Pulse Avalanche Energy ^B	E_{AS}	31	mJ
Total Power Dissipation ^B	P_D	$T_A=25^\circ\text{C}$ @ Steady State	32
		$T_A=100^\circ\text{C}$ @ Steady State	12.8
Total Power Dissipation ^B	P_D	$T_A=25^\circ\text{C}$ @ Steady State	3
		$T_A=70^\circ\text{C}$ @ Steady State	1.9
Thermal Resistance Junction-to-Ambient @ Steady State ^B	$R_{\theta JC}$	3.9	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case @ Steady State ^C	$R_{\theta JA}$	42	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
HM18DP03D	F1	HM18DP03D XXXX	5000	10000	100000	13" reel

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V, T _C =25°C			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1.0	-1.5	-2.4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -4.5V, I _D =-15A		20	25	mΩ
		V _{GS} = -10V, I _D =-8A		15	18	
		V _{GS} = -1.8V, I _D =-6.0A		20	30	
Diode Forward Voltage	V _{SD}	I _S =-18A, V _{GS} =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I _S				-1.1	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ		2992		pF
Output Capacitance	C _{oss}			330		
Reverse Transfer Capacitance	C _{rss}			272		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-9.1A		72.8		nC
Gate Source Charge	Q _{gs}			6.6		
Gate Drain Charge	Q _{gd}			10.1		
Reverse Recovery Charge	Q _{rr}	I _F =-6A, di/dt=100A/us		34		
Reverse Recovery Time	t _{rr}			67		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DS} =-15V, I _D =-6A, R _{GEN} =2.5Ω		7		ns
Turn-on Rise Time	t _r			33		
Turn-off Delay Time	t _{D(off)}			130		
Turn-off Fall Time	t _f			132		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

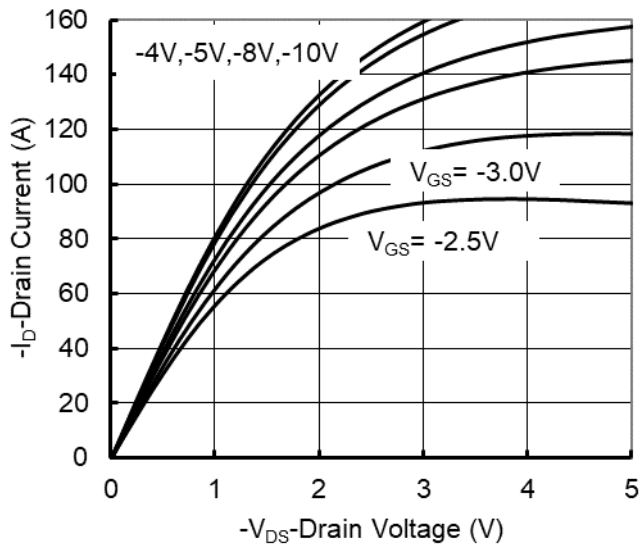


Figure 1. Output Characteristics

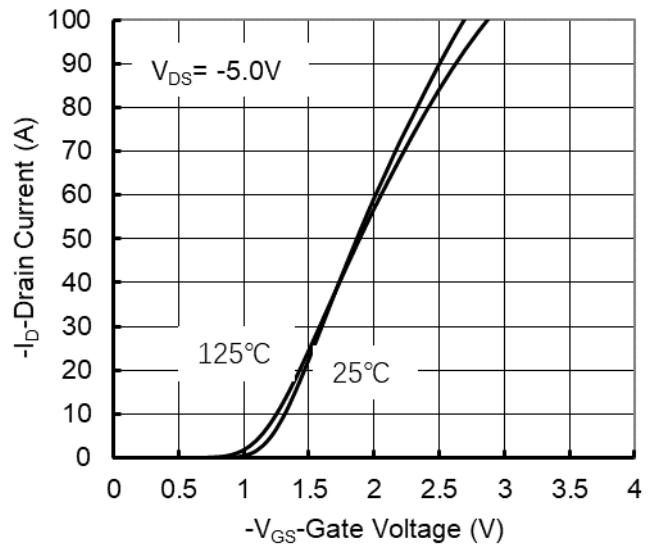


Figure 2. Transfer Characteristics

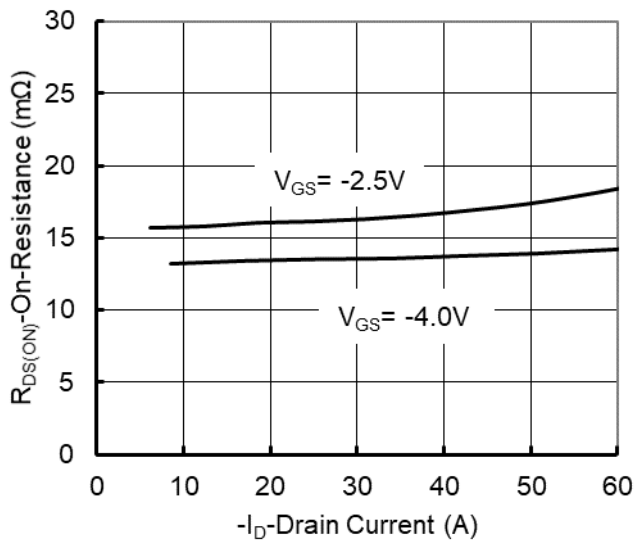


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

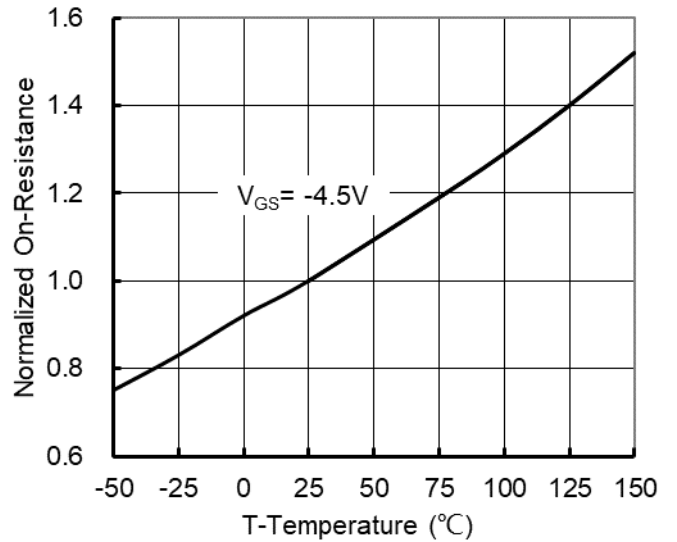


Figure 4. On-Resistance vs. Junction Temperature

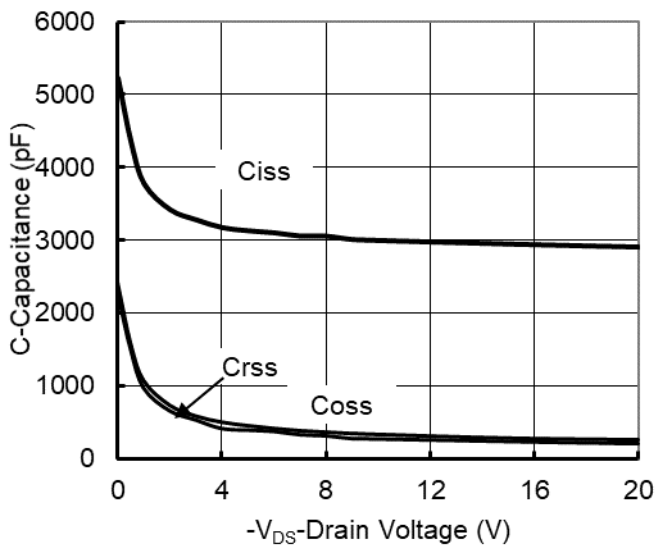


Figure 5. Capacitance Characteristics

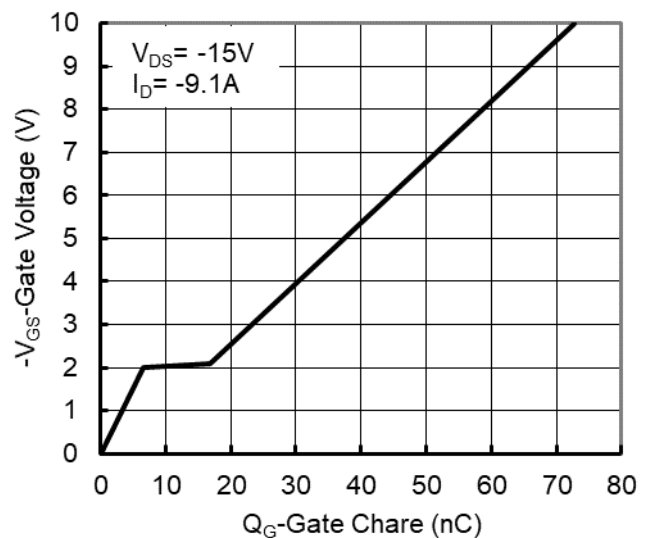


Figure 6. Gate Charge

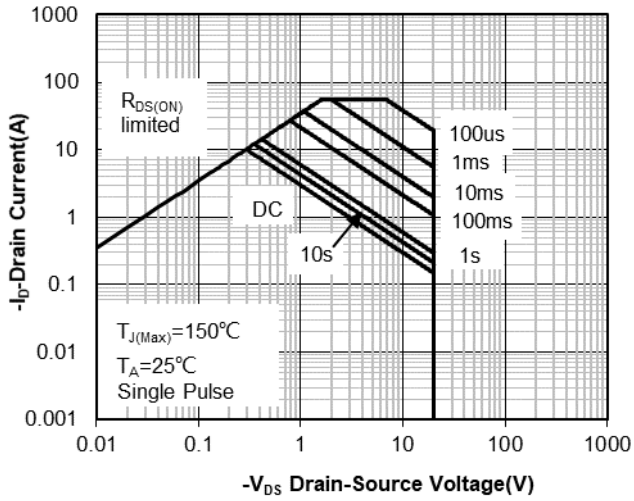


Figure 7. Safe Operation Area

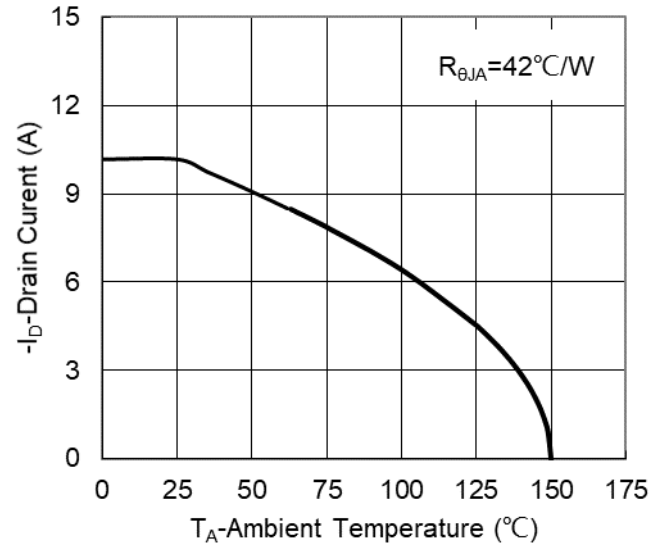


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

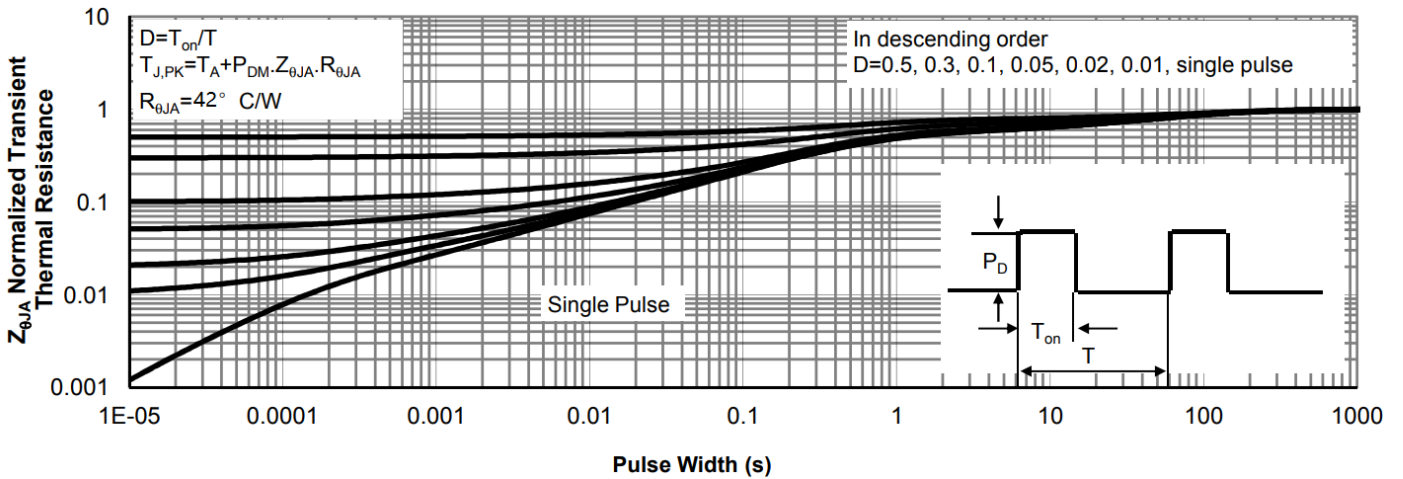
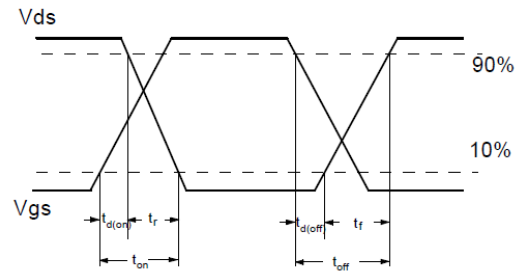
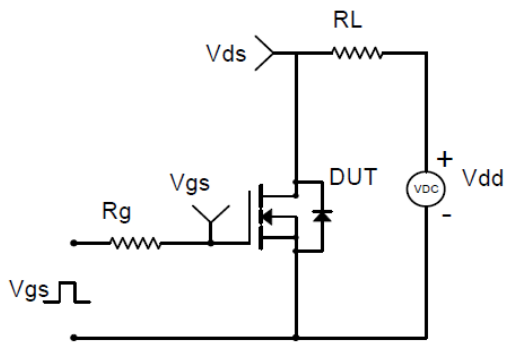
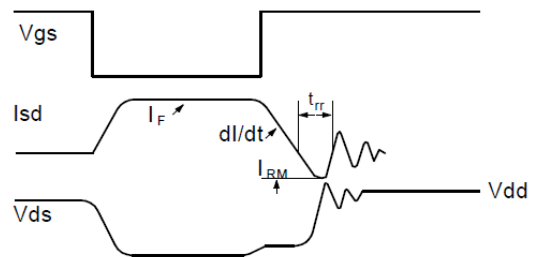
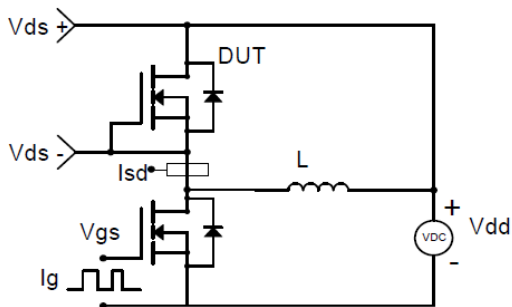


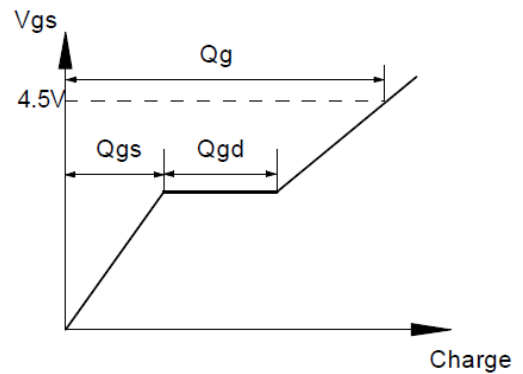
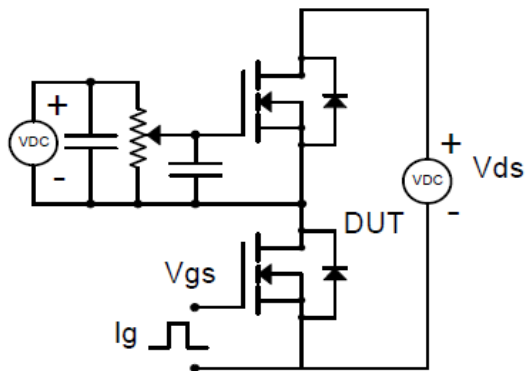
Figure 9. Normalized Maximum Transient Thermal Impedance



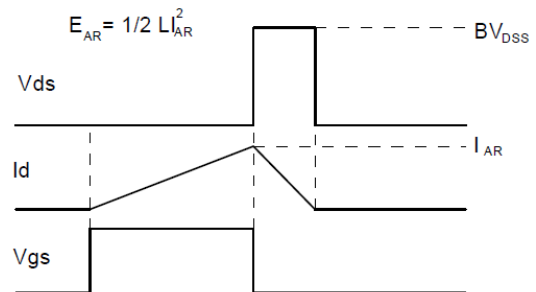
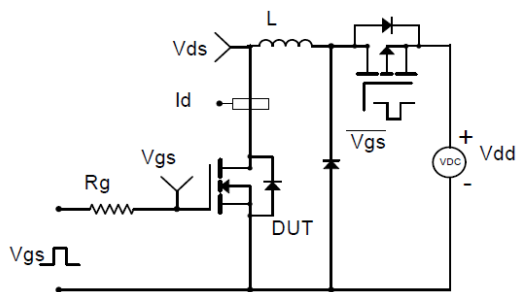
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

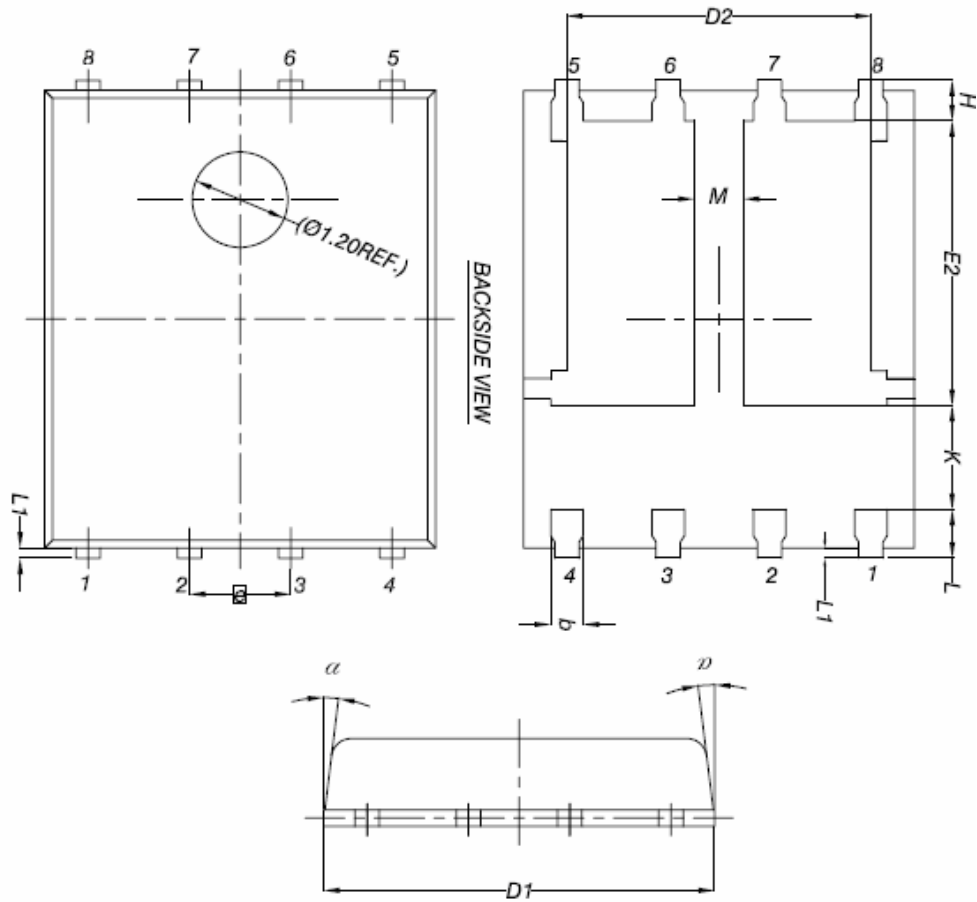


Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

DFN5X6-8L Package Information



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
α	0°	-	12°

