

N-Channel Enhancement Mode Power MOSFET

Description

The HM3207BD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in Automotive applications and a wide variety of other applications.

General Features

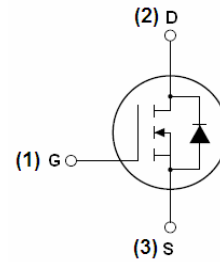
- $V_{DSS} = 70V, I_D = 180A$
 $R_{DS(ON)} < 4m\Omega @ V_{GS} = 10V$
- Good stability and uniformity with high E_{AS}
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

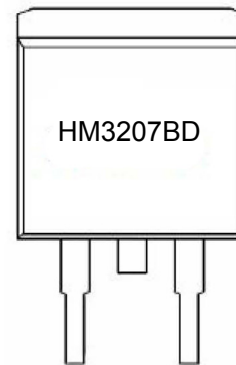
- Automotive applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

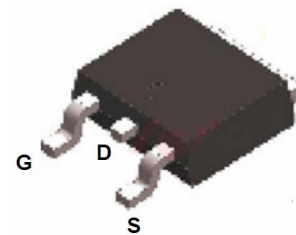
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin Assignment



TO-263-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM3207BD	HM3207BD	TO-263-2L			

Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	70	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	180	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	150	A
Pulsed Drain Current	I_{DM}	720	A
Maximum Power Dissipation	P_D	310	W
Derating factor		2.07	W/°C

Single pulse avalanche energy (Note 4)	E_{AS}	2200	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	0.48	°C/W
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	70			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=70V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 200	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A$		2.7	4	m Ω
				4.7	6.5	
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=40A$	100	165		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$		11000		PF
Output Capacitance	C_{oss}			914		PF
Reverse Transfer Capacitance	C_{rss}			695		PF
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$		23		nS
Turn-on Rise Time	t_r			190		nS
Turn-Off Delay Time	$t_{d(off)}$			130		nS
Turn-Off Fall Time	t_f			120		nS
Total Gate Charge	Q_g	$I_D=30A, V_{DD}=30V, V_{GS}=10V$	-	250		nC
Gate-Source Charge	Q_{gs}			48		nC
Gate-Drain Charge	Q_{gd}			98		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=40A$			1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 40A$ $di/dt = 100A/\mu\text{s}(\text{Note}2)$		63		nS
Reverse Recovery Charge	Q_{rr}			98		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

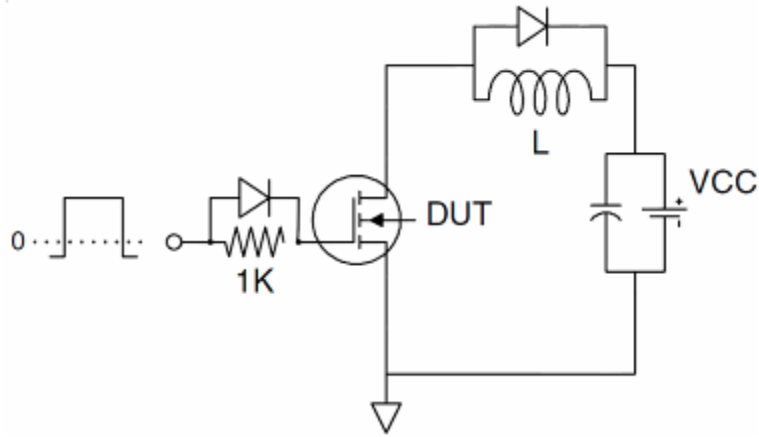
- Surface Mounted on FR4 Board, $t \leq 10$ sec.
- Pulse Test: Pulse Width $\leq 400\mu\text{s}$, Duty Cycle $\leq 2\%$.
- EAS condition: $T_J=25^\circ\text{C}, V_{DD}=37.5V, V_G=10V, L=2\text{mH}, R_G=25\Omega, I_{AS}=37A$

Test circuit

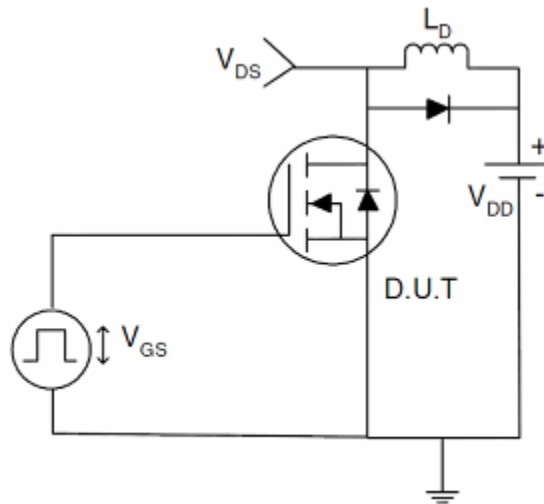
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

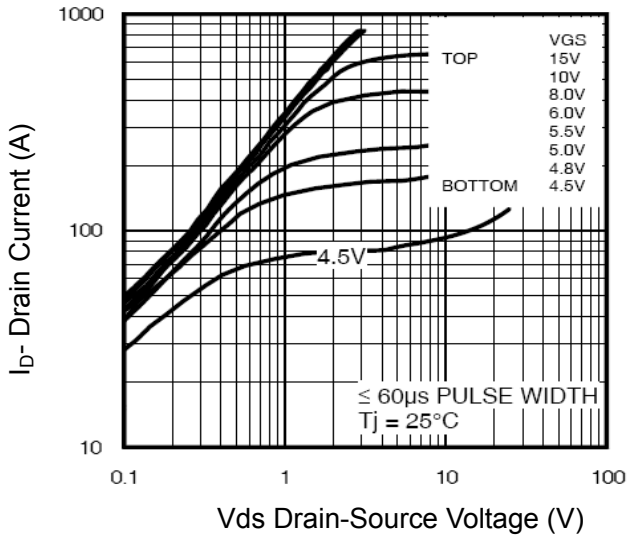


Figure 1 Output Characteristics

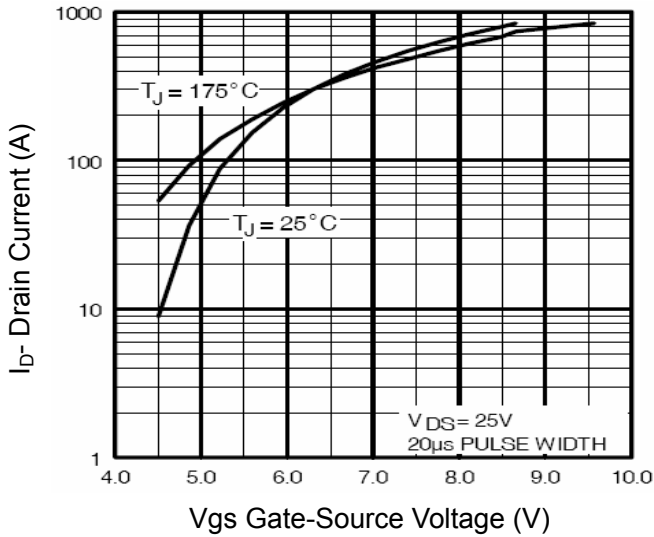


Figure 2 Transfer Characteristics

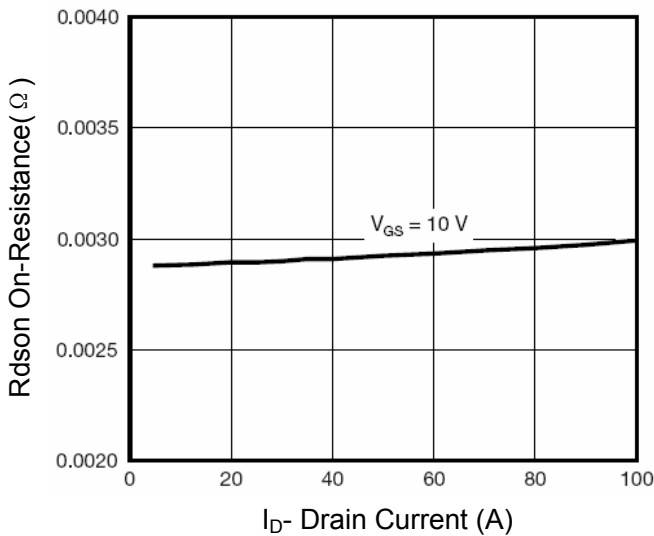


Figure 3 Rdson- Drain Current

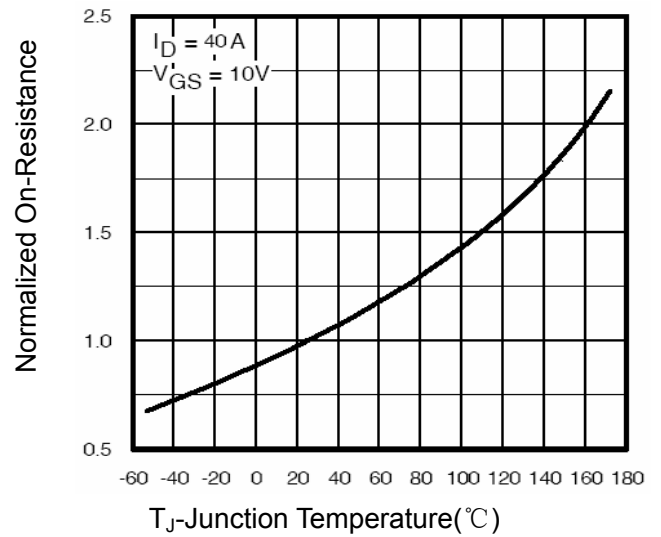


Figure 4 Rdson-Junction Temperature

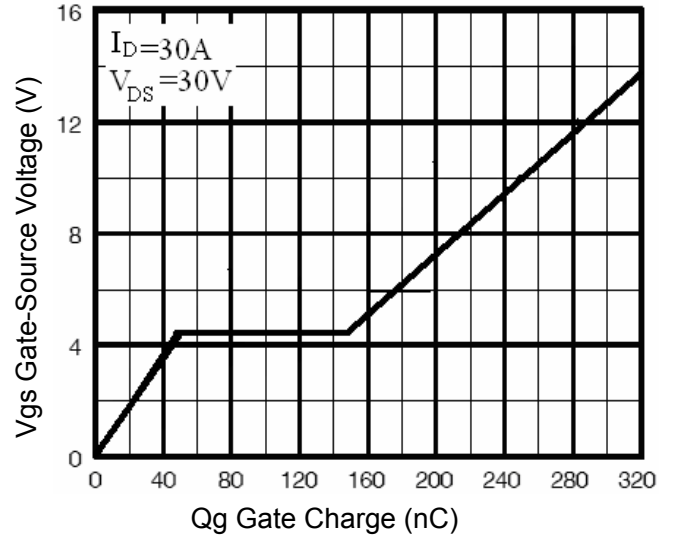


Figure 5 Gate Charge

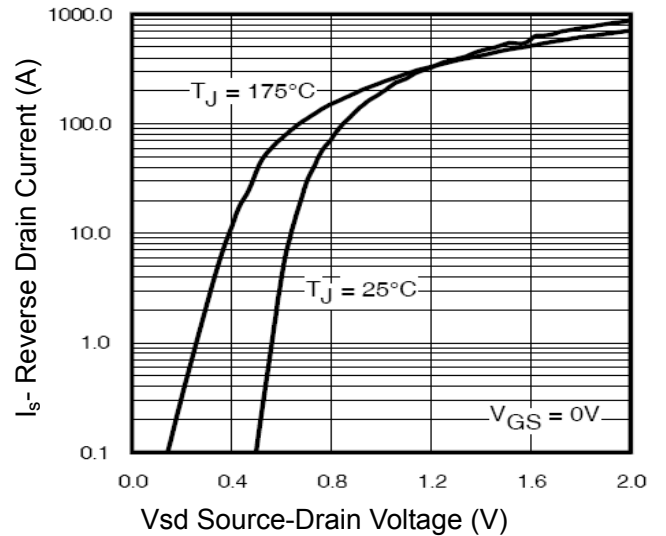


Figure 6 Source- Drain Diode Forward

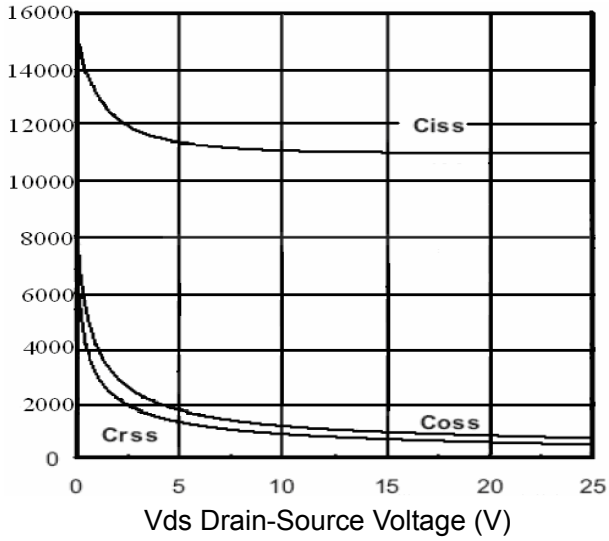


Figure 7 Capacitance vs Vds

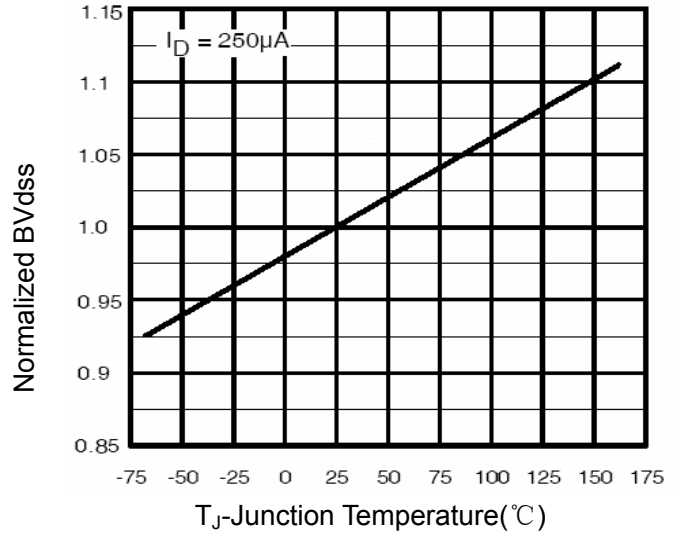


Figure 9 BV_{DSS} vs Junction Temperature

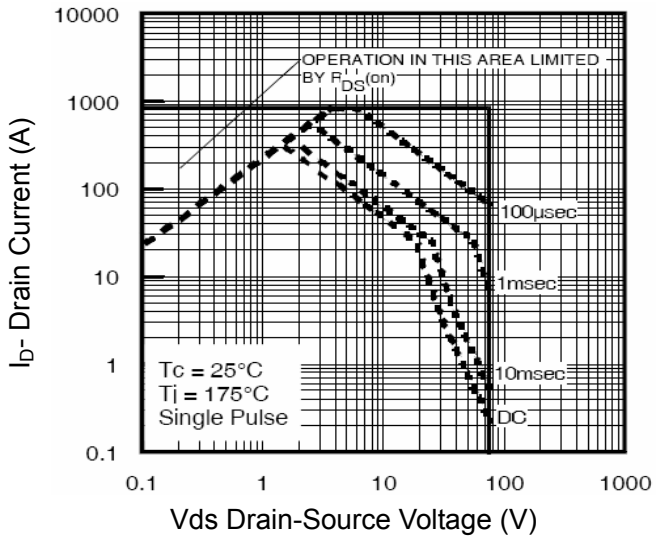


Figure 8 Safe Operation Area

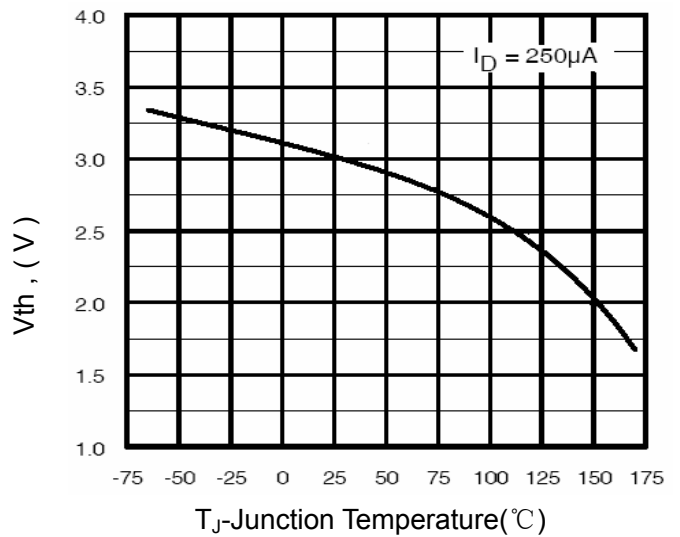


Figure 10 $V_{GS(th)}$ vs Junction Temperature

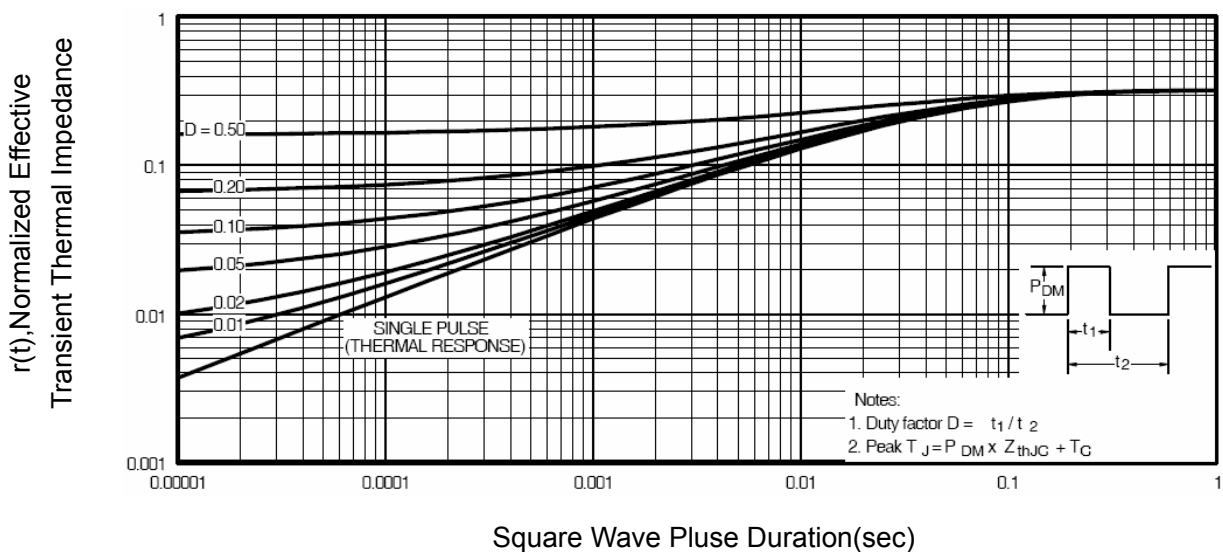
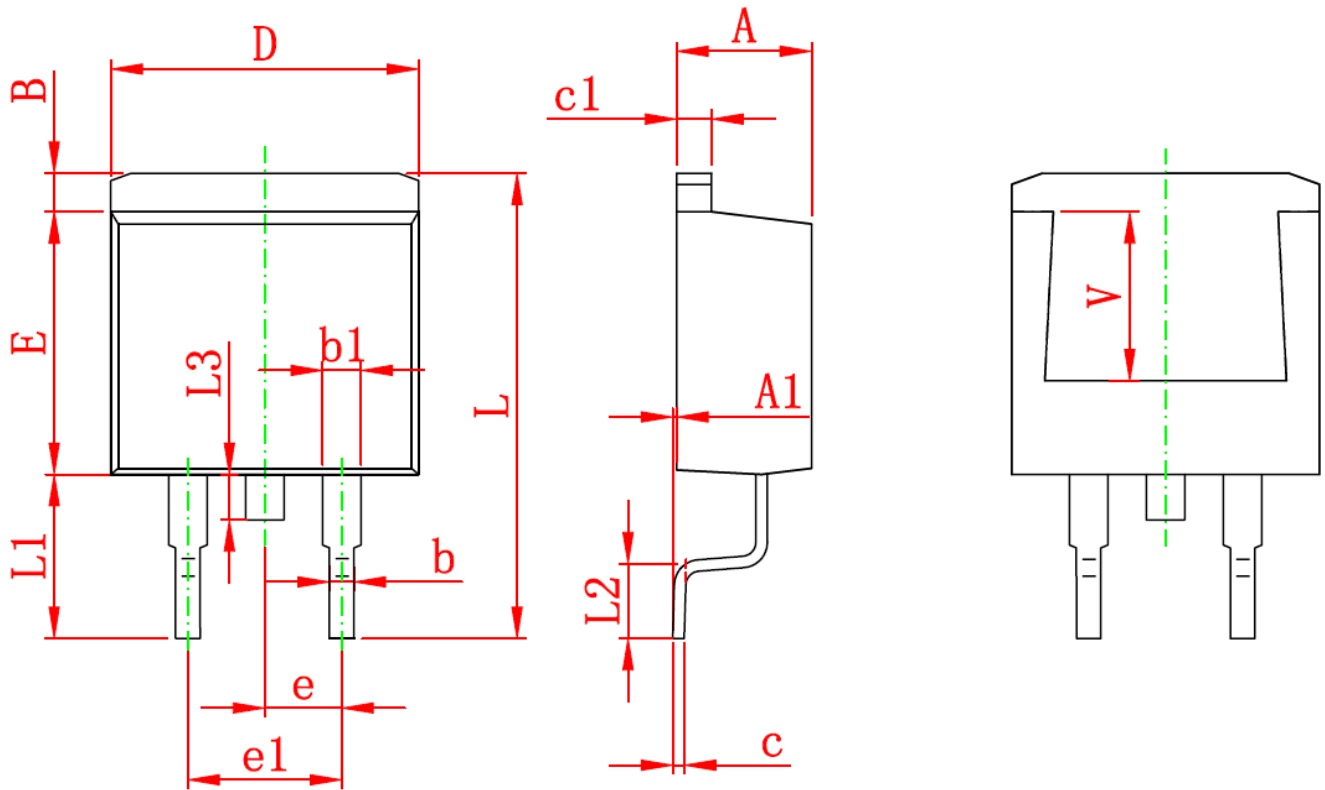


Figure 11 Normalized Maximum Transient Thermal Impedance



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.170	1.370	0.046	0.054
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 (TYP.)		0.100 (TYP.)	
e1	4.980	5.180	0.196	0.204
L	15.050	15.450	0.593	0.608
L1	5.080	5.480	0.200	0.216
L2	2.340	2.740	0.092	0.108
L3	1.300	1.700	0.051	0.067
V	5.600 REF.		0.220 REF.	