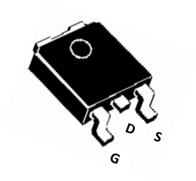
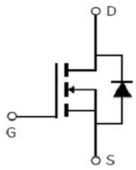
HM250N03KA

30V N-Channel MOSFET

ID(max) = 250A ,
BVDSS = 30V ,
RDS(on) = 1.2 mΩ @VGS = 10 V
RDS(on) = 2.5 mΩ @VGS = 4.5 V



TO-252



Schematic diagram

Features

- Low on-state resistance
- Fast switching
- Improved dv/dt capability
- 100% EAS tested
- Low gate charge
- High quality passivation to improve Reliability.

General Description

These N-Channel enhancement mode power field effect transistors are produced using WanToon's DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency AC-DC power switching, LED lighting, motor control and a wide variety of other applications.

Absolute max Ratings(TJ = 25°C unless otherwise noted)

Symbol	Parameter	Units	Maximum
V_{DS}	Drain-to-Source Voltage	V	30
V_{GS}	Gate-to-Source Voltage	V	±20
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V ①	A	250
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V ①	A	175
I_{DM}	Pulsed Drain Current②	A	750
E_{AS}	Single Pulse Avalanche Energy ③	mJ	400
I_{AS}	Avalanche Current ③	A	250
P_D	Power Dissipation ①	W	80.7
T_J	Operating Junction Temperature Range	℃	-50 to 150
T_{STG}	Storage Temperature Range	℃	-50 to 150

Thermal Characteristics

$R_{\theta JC}$	Maximum Junction-to-Case④	°C/W	1.55
$R_{\theta JA}$	Maximum Junction-to-Ambient⑤ ⑥	°C/W	20

Electrical characteristics(TJ = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Units	Min.	Typ.	Max.
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	V	30	—	—
$V_{(BR)DSS}/\Delta T_J$	Zero Gate Voltage Drain Current	I_D=250μA, V_{GS}=0V	V/ ℃	—	0.001	—

$R_{DS(on)}$	StaticDrain-to-Source On-resistance	V_{GS}=10V,I_D =80A	mΩ	—	1.2	1.6
		V_{GS}=4.5V,I_D =50A	mΩ	—	2.5	2.9
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	V	1.0	1.5	2.0
I_{DSS}	Drain-to-Source Leakage Current	V_{DS} = 30V,V_{GS} = 0V	μA	—	—	1
I_{GSS}	Gate-to-Source forward leakage	V_{GS} =20V	nA	—	—	100
		V_{GS} = -20V		—	—	-100
V_{SD}	Diode Forward Voltage	I_S=90A, V_{GS}=0V	V	0.3	0.8	1.2

Dynamic characteristics(TJ = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Units	Min.	Typ.	Max.
R_g	Gate Resistance	V_{GS} = 0V,V_{DS} = 0V,f = 1MHz	Ω	—	2.5	—
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 15V f = 1MHz	pF	—	4523	—
C_{oss}	Output Capacitance			—	801	—
C_{rss}	Reverse Transfer Capacitance			—	644	—
Q_g	Total Gate Charge	I_D =90A, V_{DS}=15V, V_{GS} =10V	nC	—	100	—
Q_{gs}	Gate-to-Source Charge			—	15	—
Q_{gd}	Gate-to-Drain("Miller") Charge			—	10.1	—
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DD}=15V, I_D=90A, R_G=2.2Ω	ns	—	15.1	—
t_r	Turn-On Rise Time			—	80	—
$t_{D(off)}$	Turn-Off DelayTime			—	56	—
t_f	Turn-Off Fall Time			—	36	—
t_{rr}	Body Diode Reverse Recovery Time	I_F=90A, dI/dt=500A/μs	ns	—	19.6	—
Q_{rr}	Body Diode Reverse Recovery Charge		nC	—	10.3	—

①Based on $T_{J(MAX)}$=150℃ in a TO-252 package, using junction-to-case thermal resistance.
②Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃.
③L=0.5mH, I_{AS}=10A, V_{DD}=15V, R_G=3Ω, Starting T_J=25℃.
④These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heat sink, assuming a maximum junction temperature of $T_{J(MAX)}$=150℃.
⑤The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
⑥These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃.

Typical electrical and thermal characteristics：

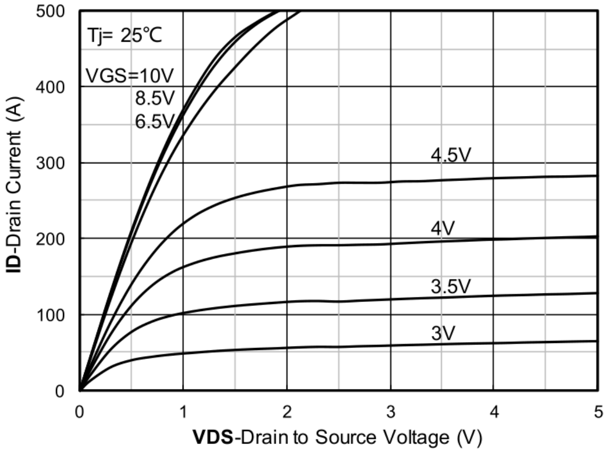


Figure 1: Typical Output Characteristics

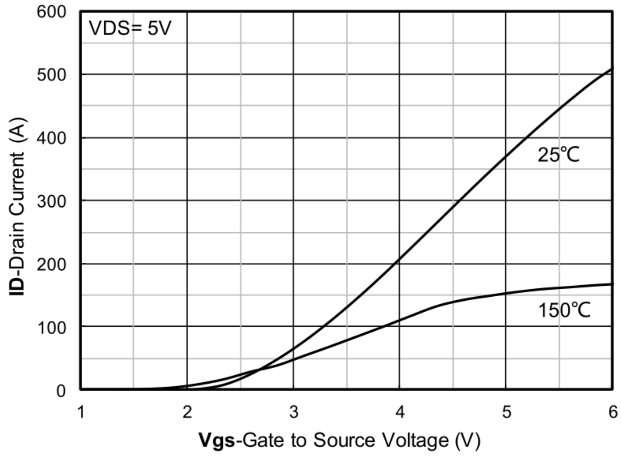


Figure 2: Typical Transfer Characteristics

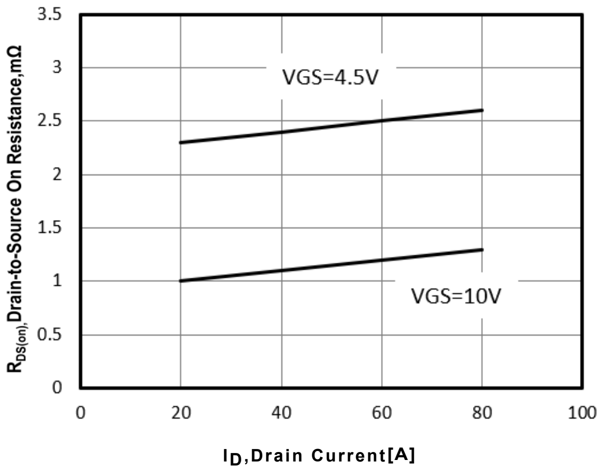


Figure 3: Drain-to-Source On Resistance vs Drain Current

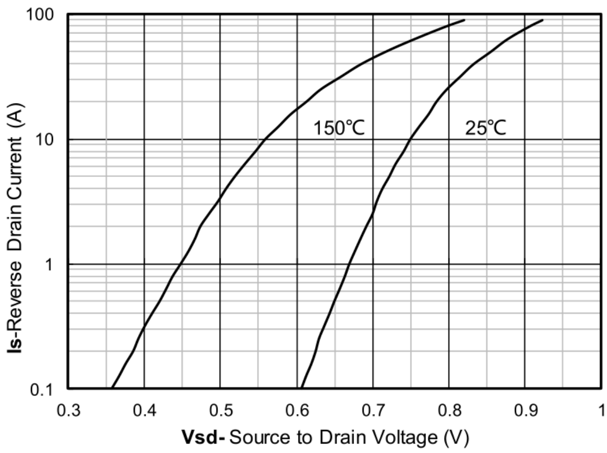


Figure 4: Typical Body Diode Transfer Characteristics

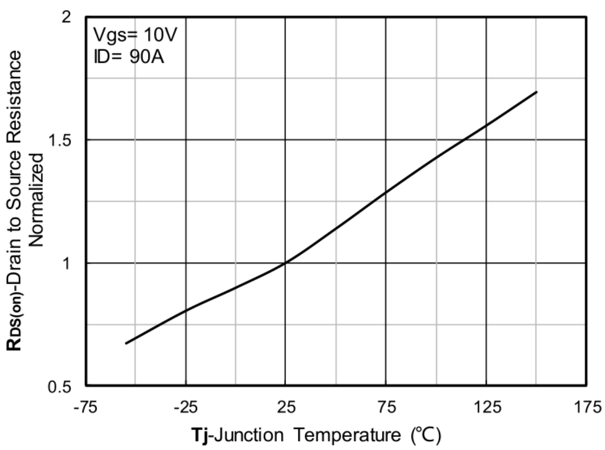


Figure 5: Normalized On Resistance vs Junction Temperature

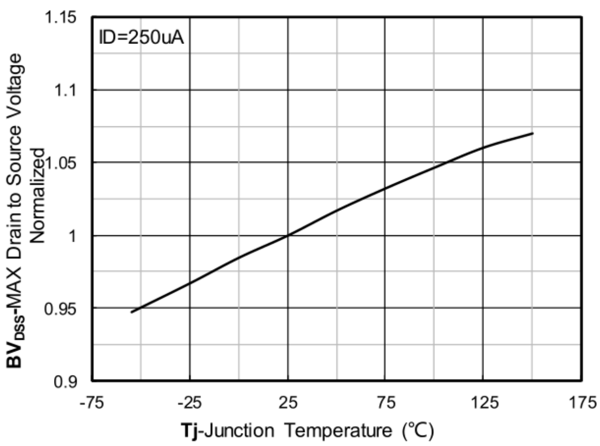


Figure 6: Normalized Breakdown Voltage vs Junction Temperature

Typical electrical and thermal characteristics：

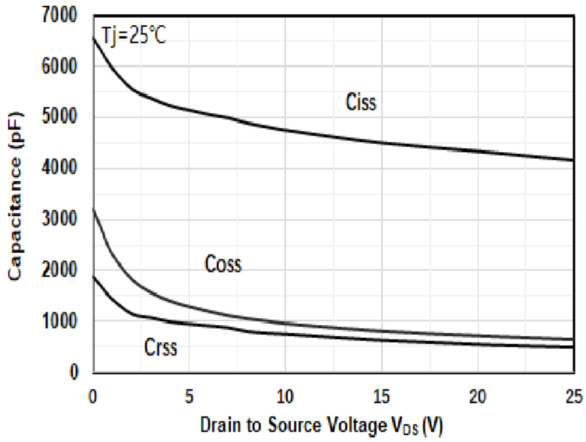


Figure 7: Capacitance Characteristics

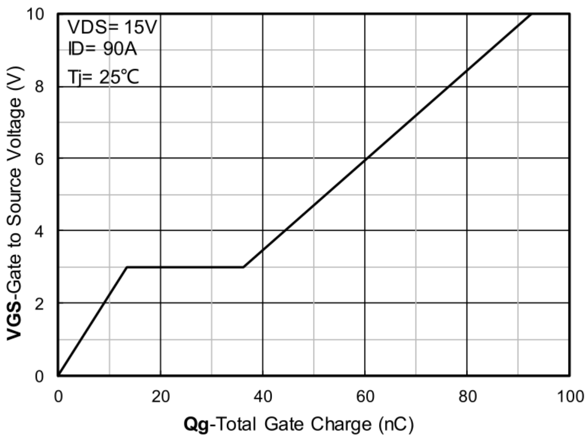


Figure 8: Typical Gate Charge vs Gate to Source Voltage

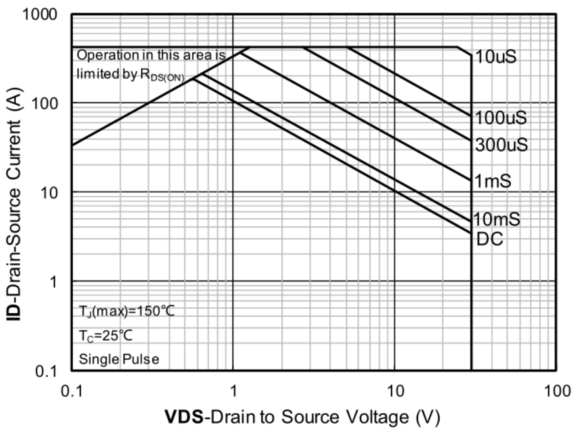


Figure 9: Maximum Safe Operating Area

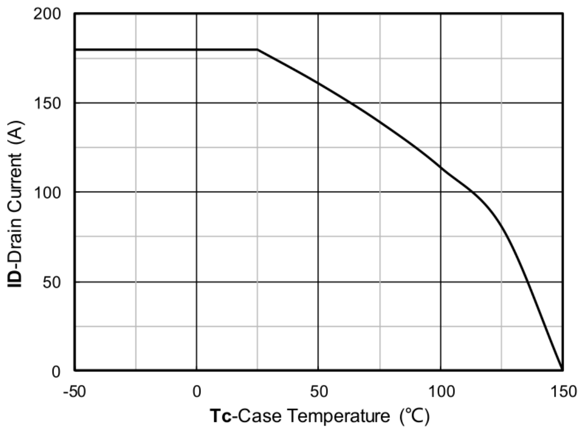


Figure 10: Maximum Continuous Drain Current vs Case Temperature

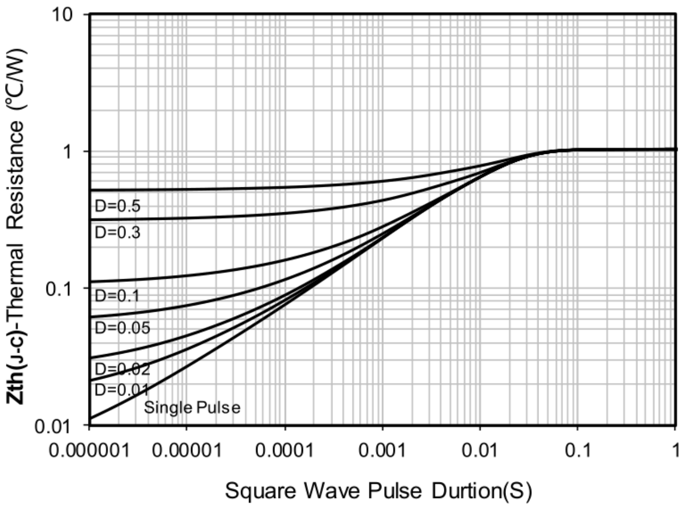


Figure 11: Maximum Effective Thermal Impedance , Junction to Case

Test Circuit and Waveforms:

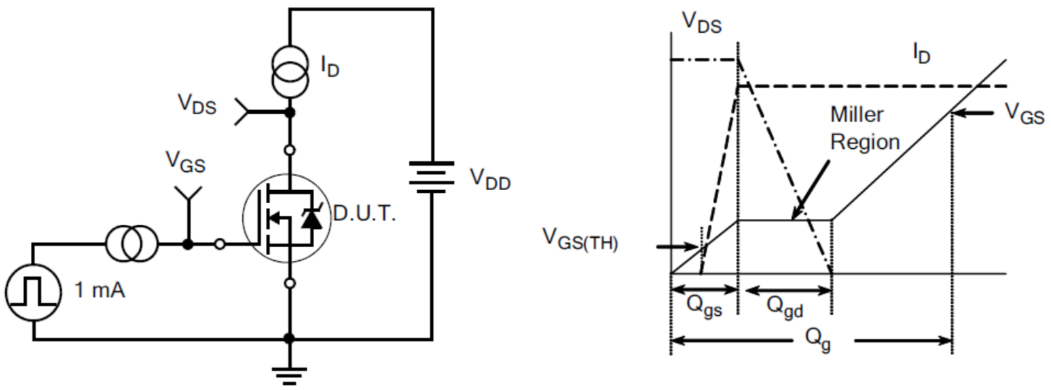


Figure 12: Gate Charge Test Circuit and Waveform

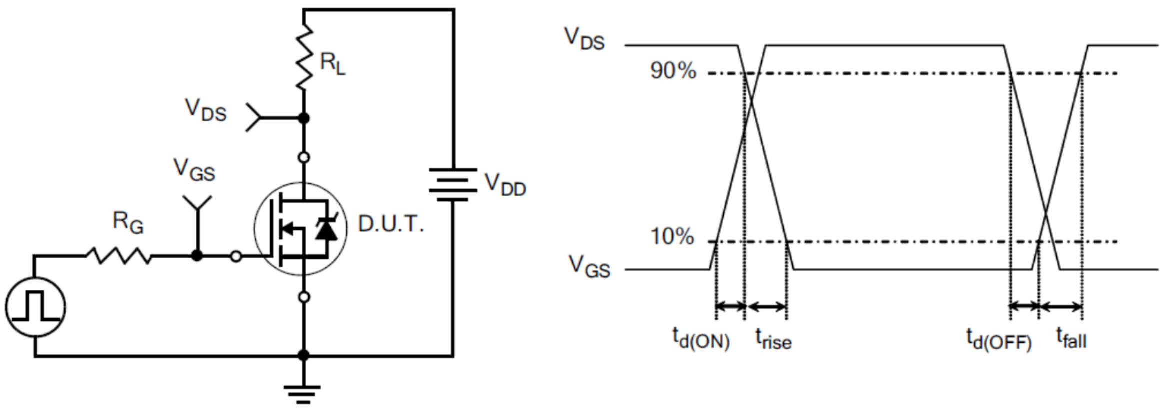


Figure 13: Switching time test circuit and waveform

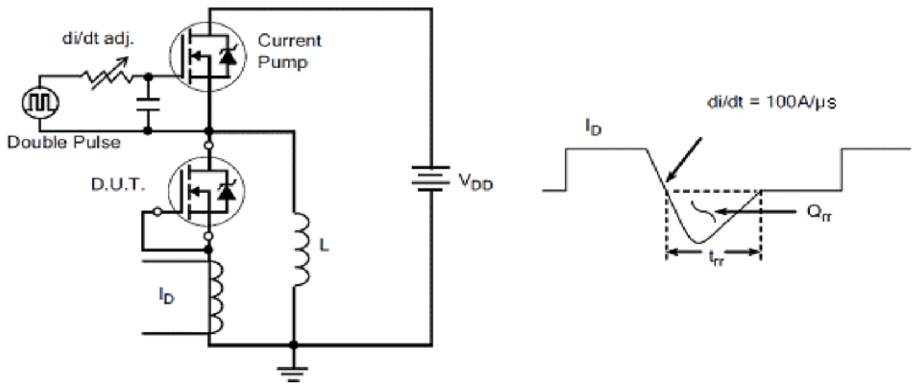


Figure 14: Reverse Recovery Test Circuit and Waveform

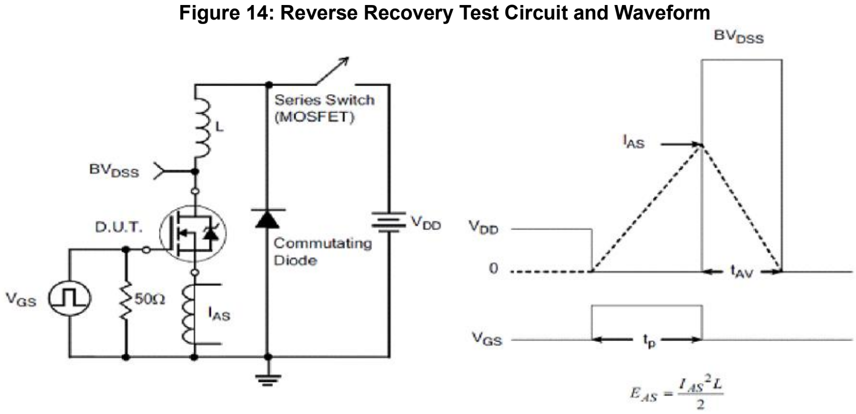
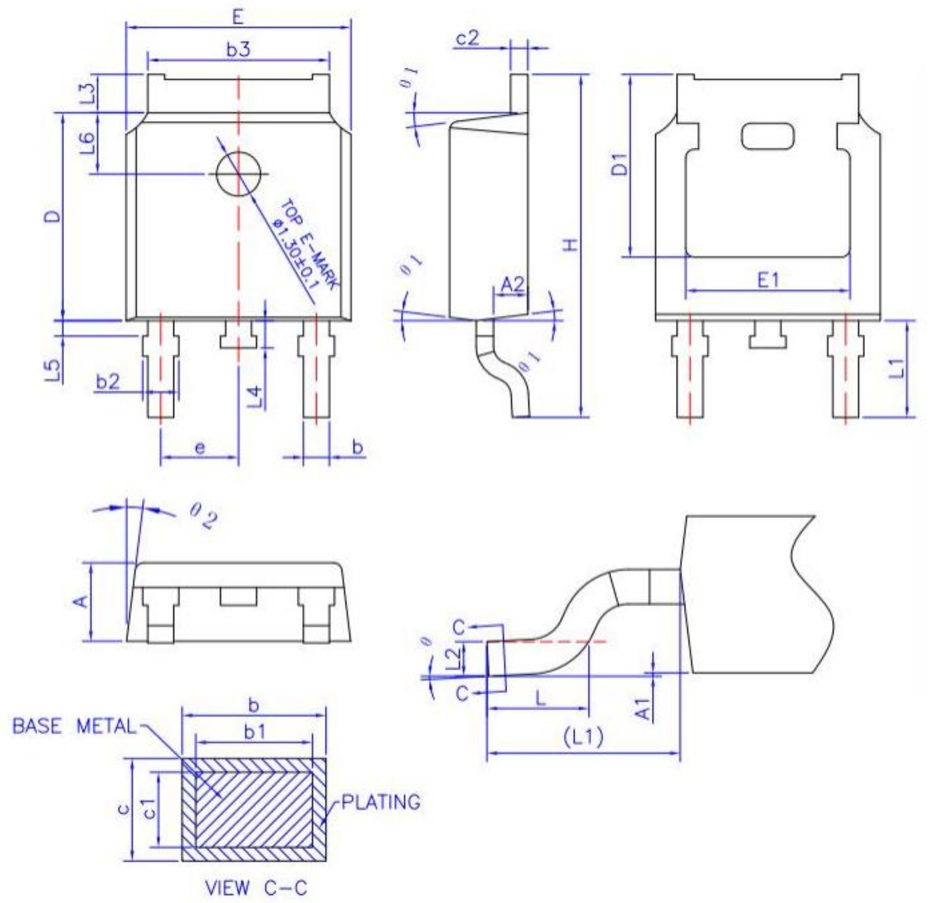


Figure 15: Avalanche Test Circuit and Waveform

Mechanical Data：TO-252



SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0	---	0.10
A2	0.90	1.01	1.10
b	0.72	---	0.85
b1	0.71	0.76	0.81
b2	0.72	---	0.90
b3	5.13	5.33	5.46
c	0.47	---	0.60
c1	0.46	0.51	0.56
c2	0.47	---	0.60
D	6.00	6.10	6.20
D1	5.25	---	---
E	6.50	6.60	6.70
E1	4.70	---	---
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.508 BSC		
L3	0.90	---	1.25
L4	0.60	0.80	1.00
L5	0.15	---	0.75
L6	1.80 REF		
θ	0°	---	8°
θ1	5°	7°	9°
θ2	5°	7°	9°