

### Description

The HM40N02Q uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

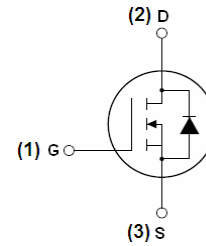
- $V_{DS} = 20V, I_D = 40A$   
 $R_{DS(ON)} < 5m\Omega @ V_{GS} = 4.5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

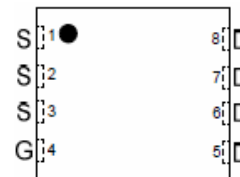
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

**100% UIS TESTED!**

**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Pin Assignment



DFN 3.3x3.3 EP top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM40N02Q	HM40N02Q	DFN3X3-8L	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous	$I_D$	40	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	28	A
Pulsed Drain Current	$I_{DM}$	120	A
Maximum Power Dissipation	$P_D$	60	W
Derating factor		0.48	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	200	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	2.1	$^\circ C/W$
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**Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)**

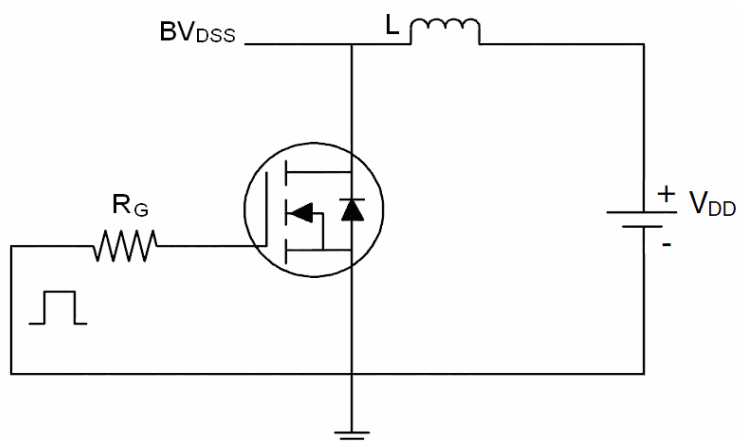
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	20	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.4	0.7	1.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =20 A	-	3.8	5.0	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =15A		4.6	7.0	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =20A	15	-	-	S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, F=1.0MHZ	-	2000	-	PF
Output Capacitance	C <sub>oss</sub>		-	500	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	200	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V, I <sub>D</sub> =2A, R <sub>L</sub> =1Ω V <sub>GS</sub> =4.5V, R <sub>G</sub> =3Ω	-	6.4	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	17.2	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	29.6	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	16.8	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	27		nC
Gate-Source Charge	Q <sub>gs</sub>		-	6.5		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	6.4		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	-		1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	40	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A di/dt = 100A/μs (Note3)	-	25	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	24	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

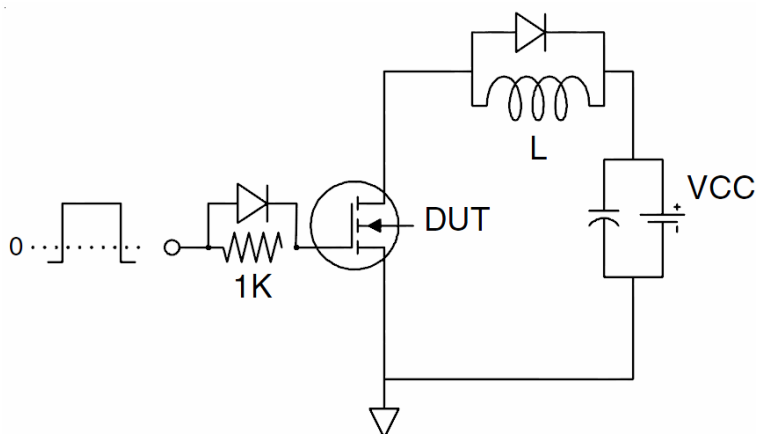
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E<sub>AS</sub> condition : T<sub>J</sub>=25°C, V<sub>DD</sub>=10V, V<sub>G</sub>=10V, L=0.5mH, R<sub>g</sub>=25Ω.

Test circuit

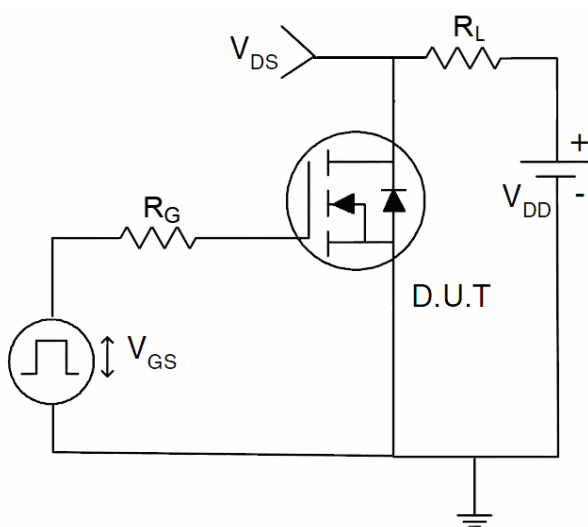
1)  $E_{AS}$  Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

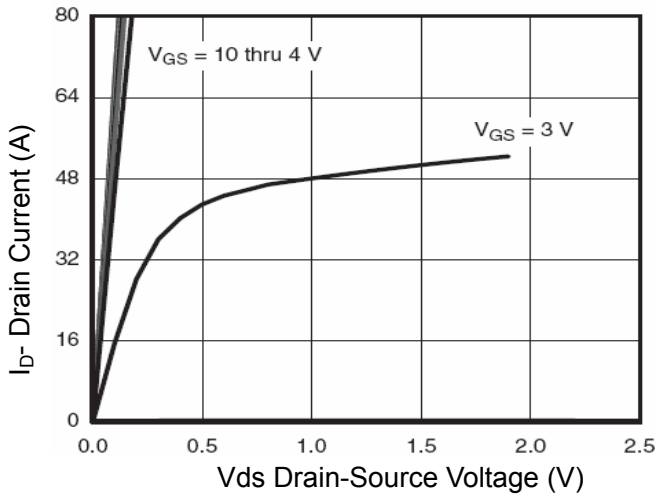


Figure 1 Output Characteristics

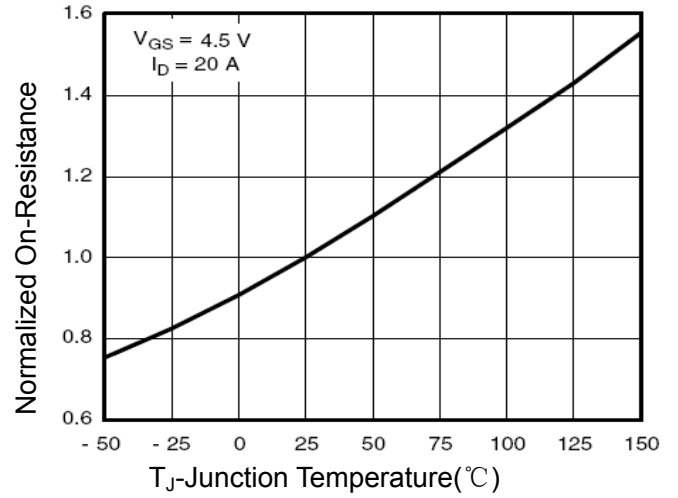


Figure 4 Rdson-Junction Temperature

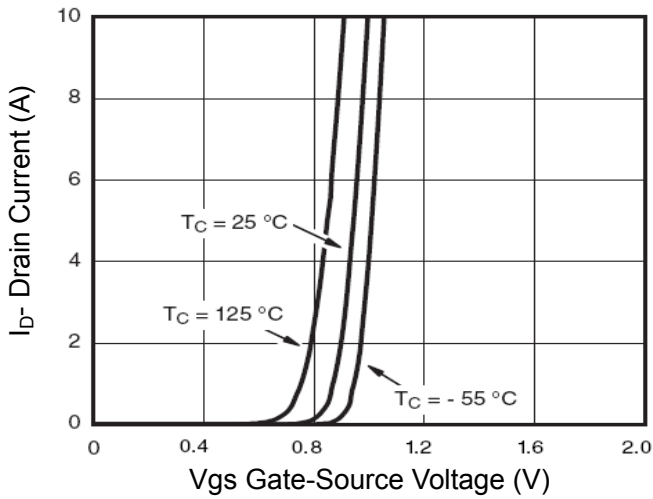


Figure 2 Transfer Characteristics

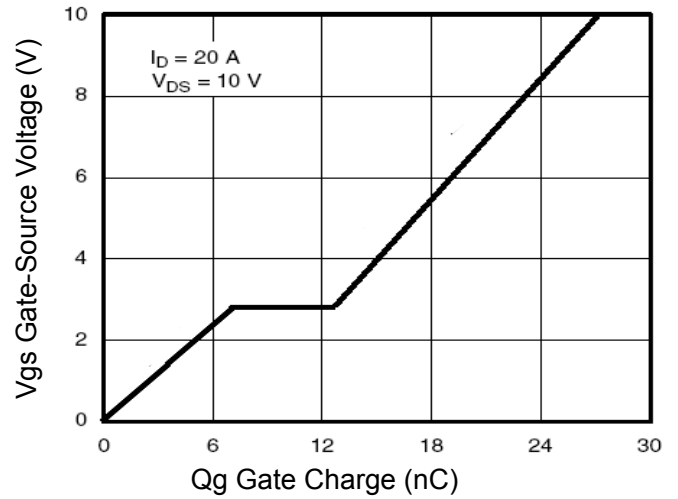


Figure 5 Gate Charge

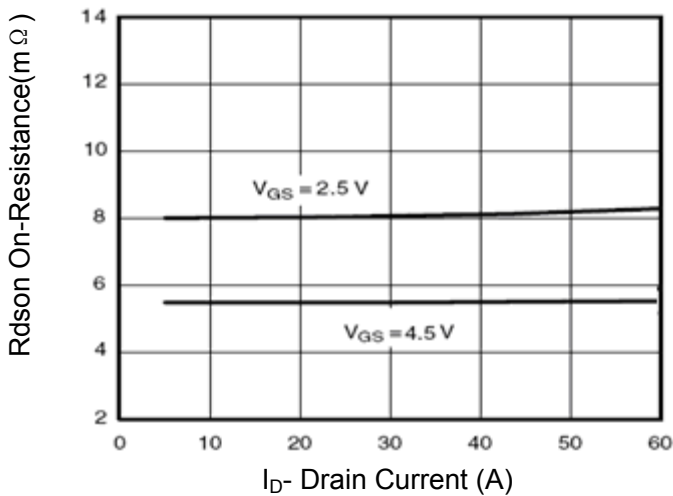


Figure 3 Rdson- Drain Current

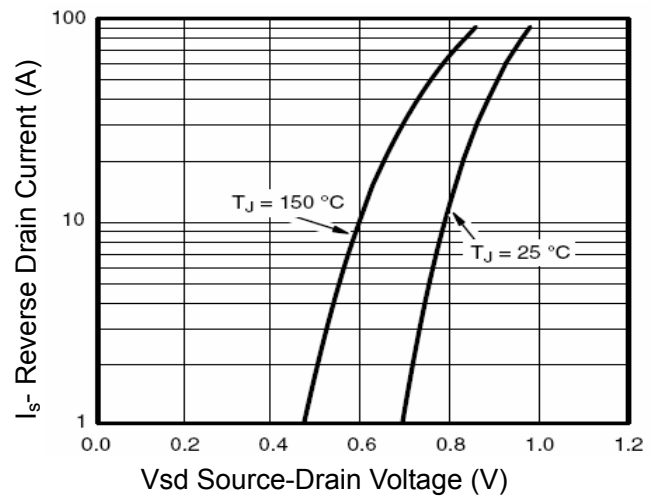


Figure 6 Source- Drain Diode Forward

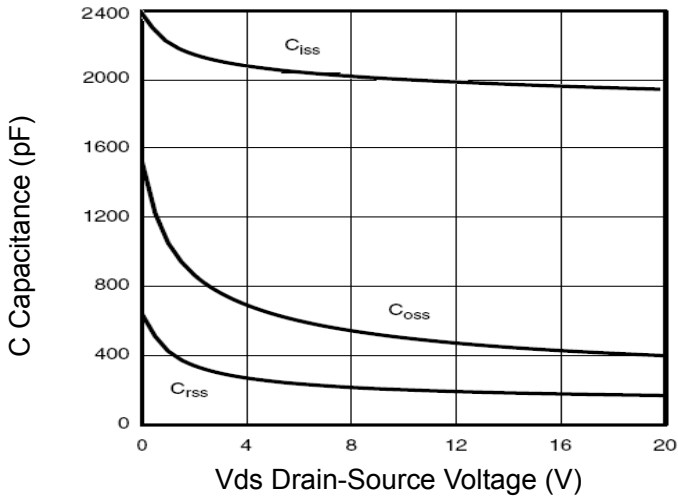


Figure 7 Capacitance vs Vds

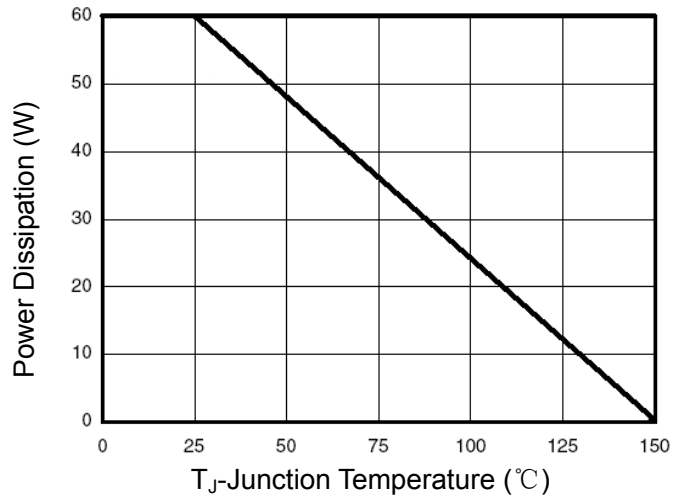


Figure 9 Power De-rating

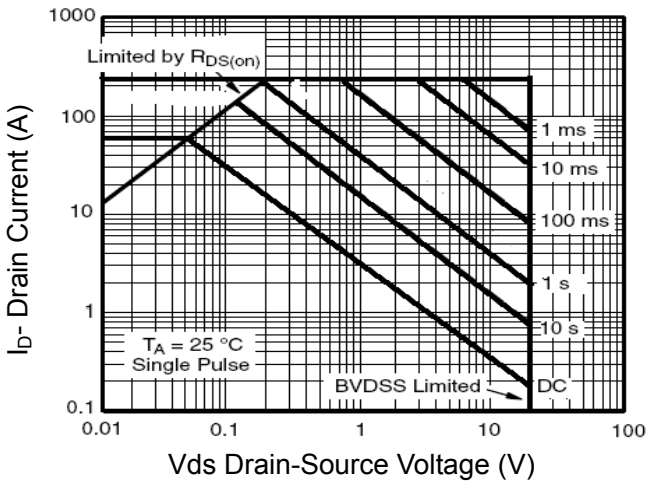


Figure 8 Safe Operation Area

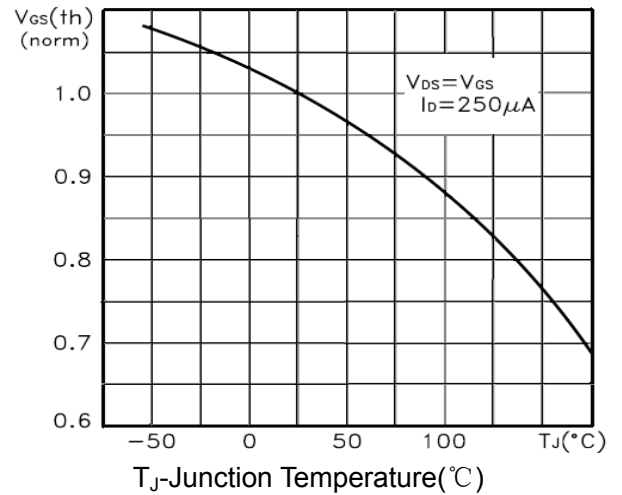


Figure 10  $V_{GS(th)}$  vs Junction Temperature

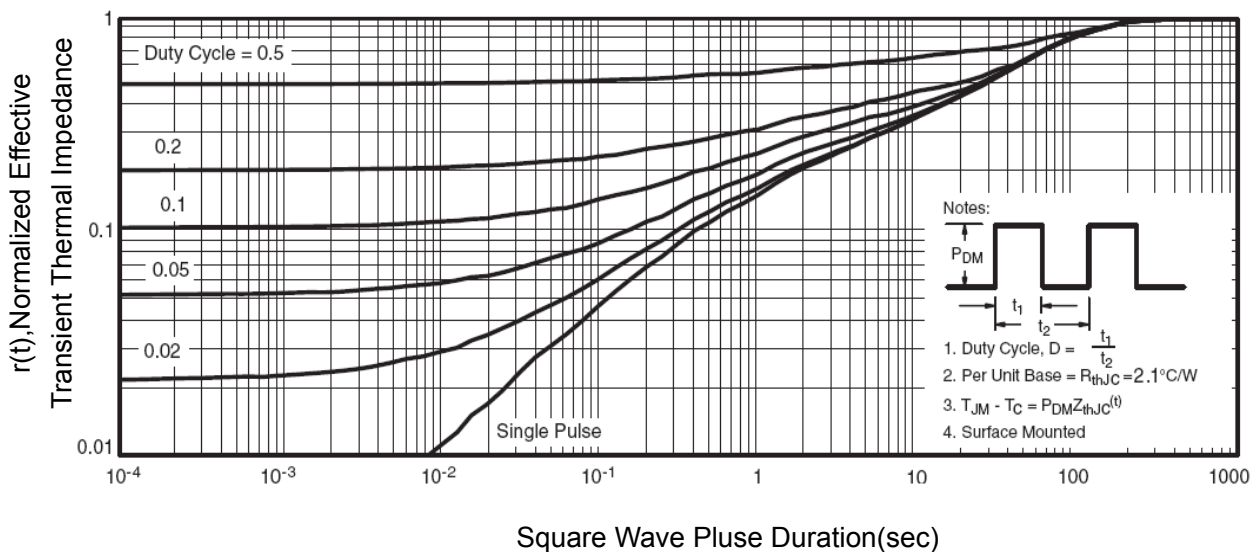
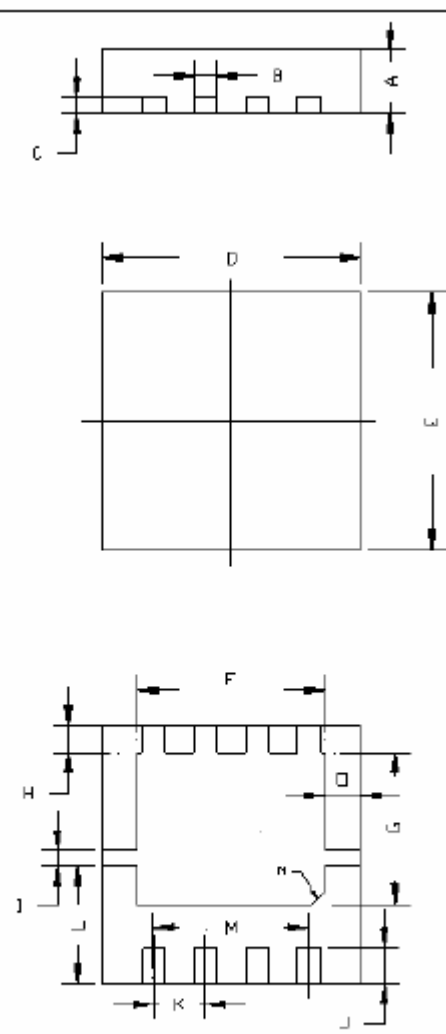


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3.3X3.3 EP Package Information

封装外形尺寸图				
	符号	单位: mm		
		MIN	MAX	TYP
	A	0.75	0.85	0.8
	B	0.25	0.35	0.3
	C	0.18	0.22	0.2
	D	3.2	3.3	3.25
	E	3.2	3.3	3.25
	F	2.2	2.5	2.35
	G	1.8	2.0	1.9
	H	0.3	0.4	0.35
	I	0.15	0.25	0.2
	J	0.4	0.5	0.45
	K	0.6	0.7	0.65
	L	1.38	1.58	1.48
	M	1.8	2.1	1.95
	N	0.15*45°		
	O	0.4	0.5	0.45