

## Dual N-Channel Enhancement Mode Power MOSFET

### DESCRIPTION

The HM4828A uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

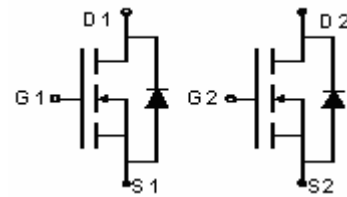
### GENERAL FEATURES

- $V_{DS} = 60V, I_D = 4.5A$   
 $R_{DS(ON)} < 35m\Omega @ V_{GS} = 10V$  (Typ. 26m $\Omega$ )  
 $R_{DS(ON)} < 45m\Omega @ V_{GS} = 4.5V$  (Typ. 32m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized Avalanche voltage and current
- Low Gate to Drain Charge to Reduce Switching Losses

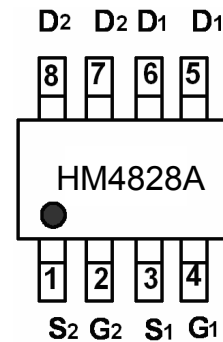
### Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

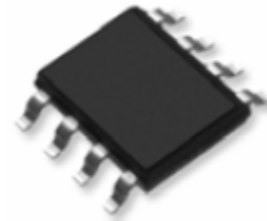
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin Assignment



SOP-8 top view

### Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM4828A	HM4828A	SOP-8	Ø330mm	12mm	2500 units

### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	±20	V
Drain Current-Continuous	$I_D$	4.5	A
Drain Current-Continuous( $T_C=100^\circ C$ )	$I_D(100^\circ C)$	3.0	A
Pulsed Drain Current	$I_{DM}$	24	A
Maximum Power Dissipation	$P_D$	2	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	62.5	°C/W
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**Electrical Characteristics (TA=25°C unless otherwise noted)**

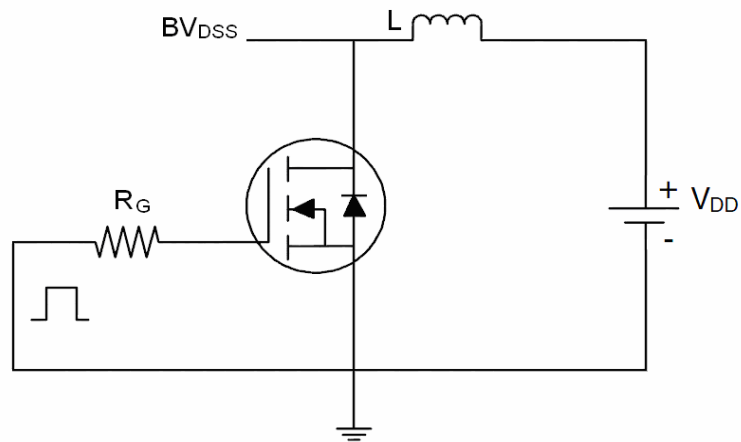
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	69	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	2	3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4.5A$		26	35	
		$V_{GS}=4.5V, I_D=3A$	-	32	45	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=4.5A$	11	-	-	S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$		450		PF
Output Capacitance	$C_{oss}$			60		PF
Reverse Transfer Capacitance	$C_{rss}$			25		PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DS}=30V, I_D=4.5A$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	4.7	-	nS
Turn-on Rise Time	$t_r$		-	2.3	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	15.7	-	nS
Turn-Off Fall Time	$t_f$		-	1.9	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=30V, I_D=4.5A,$ $V_{GS}=10V$	-	8.5	-	nC
Gate-Source Charge	$Q_{gs}$		-	1.6	-	nC
Gate-Drain Charge	$Q_{gd}$		-	2.2	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=3.7A$	-	-	1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	4	A

**Notes:**

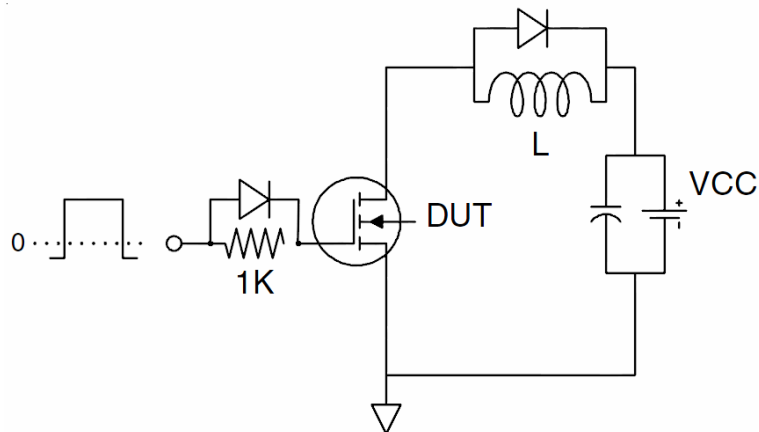
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

## Test circuit

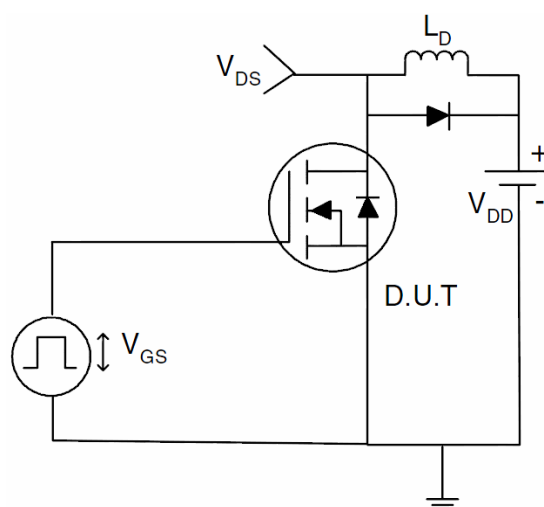
### 1) $E_{AS}$ test Circuits



### 2) Gate charge test Circuit:



### 3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

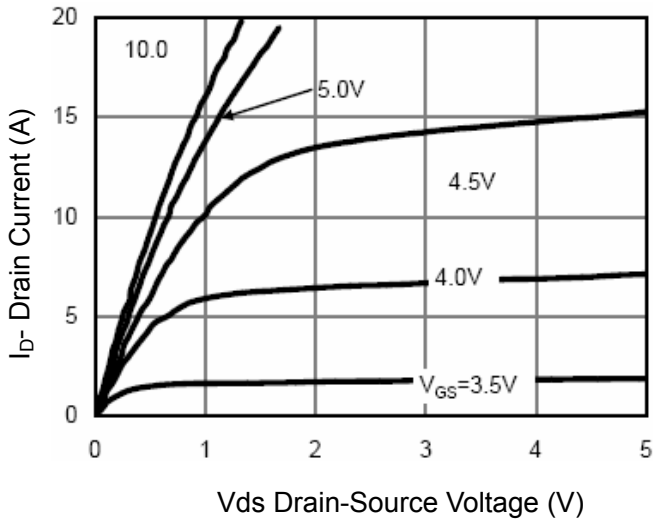


Figure 1 Output Characteristics

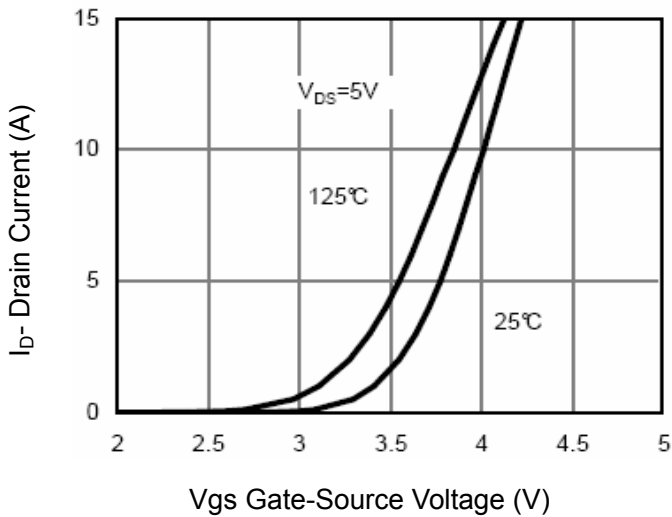


Figure 2 Transfer Characteristics

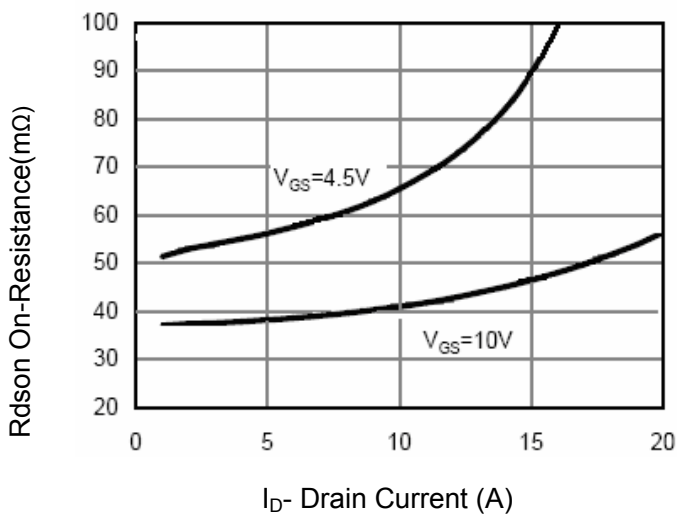


Figure 3 Rdson- Drain Current

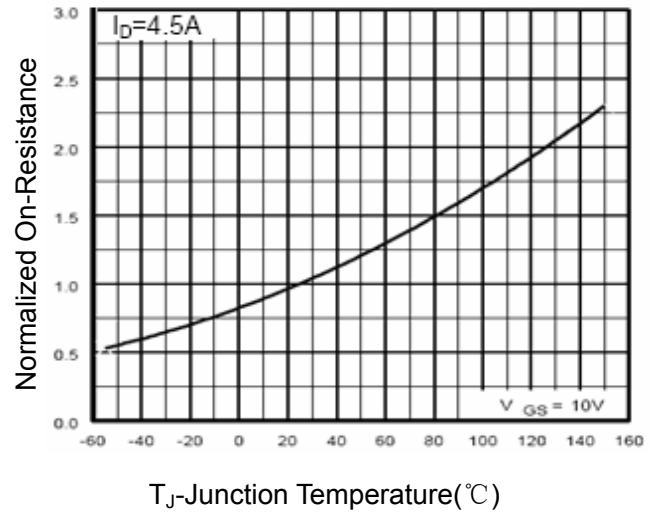


Figure 4 Rdson-Junction Temperature

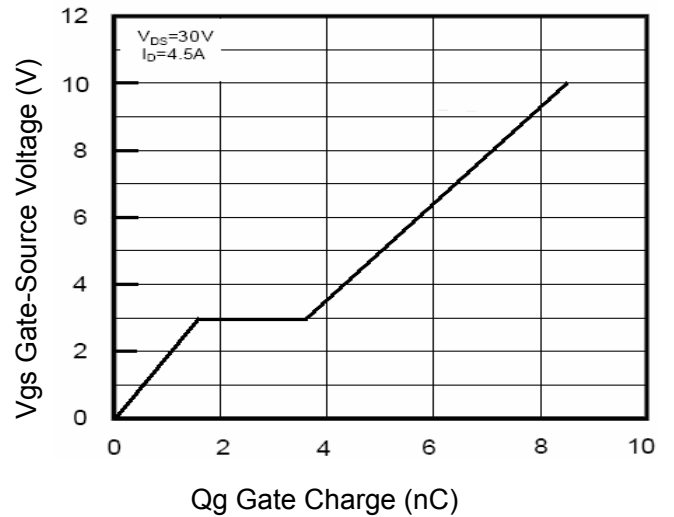


Figure 5 Gate Charge

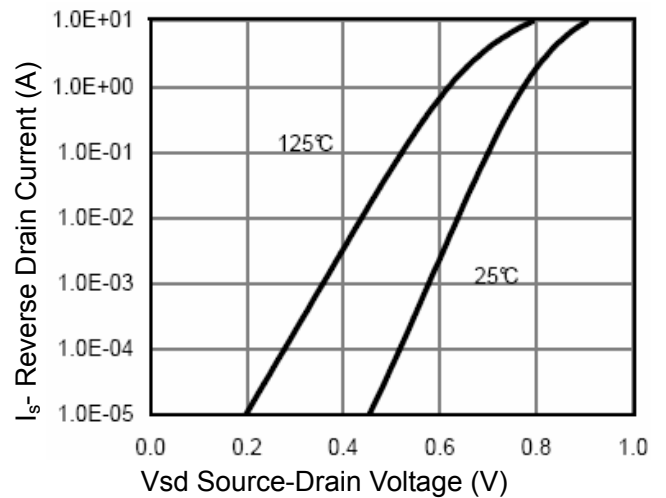


Figure 6 Source- Drain Diode Forward

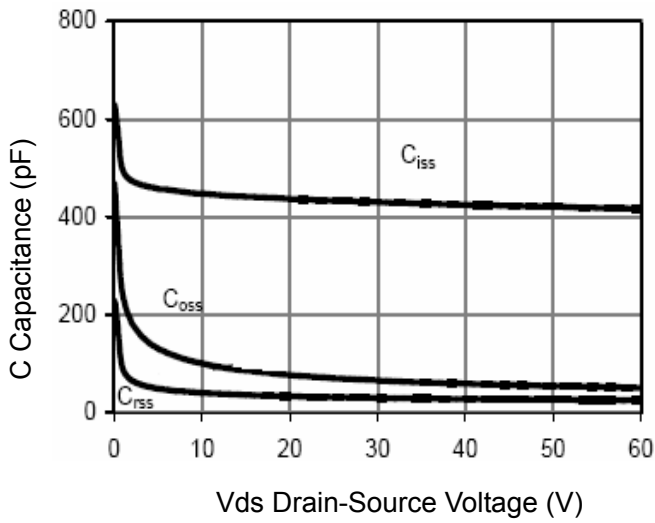


Figure 7 Capacitance vs Vds

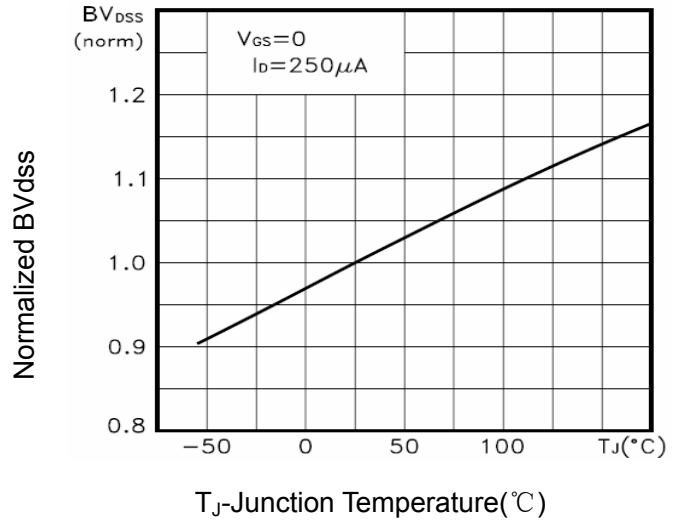


Figure 9  $BV_{DSS}$  vs Junction Temperature

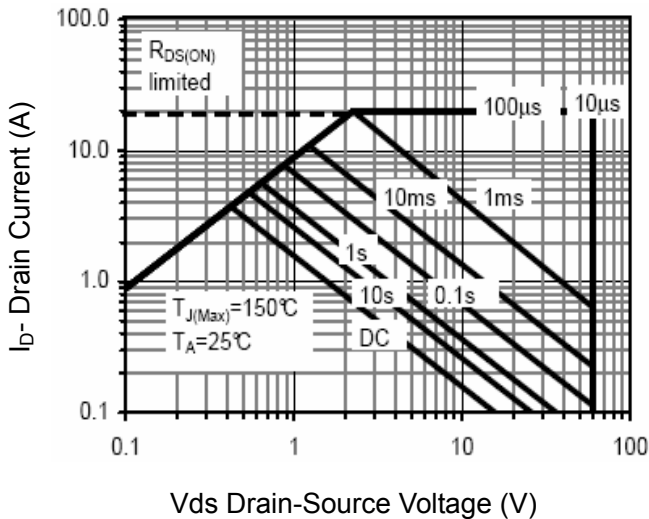


Figure 8 Safe Operation Area

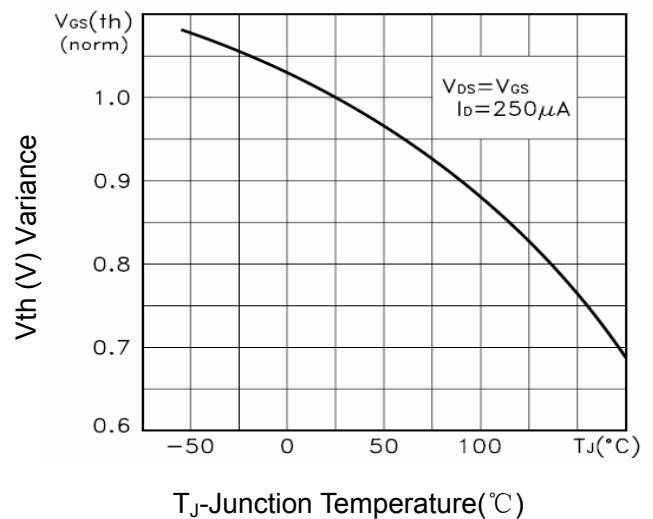


Figure 10  $V_{GS(th)}$  vs Junction Temperature

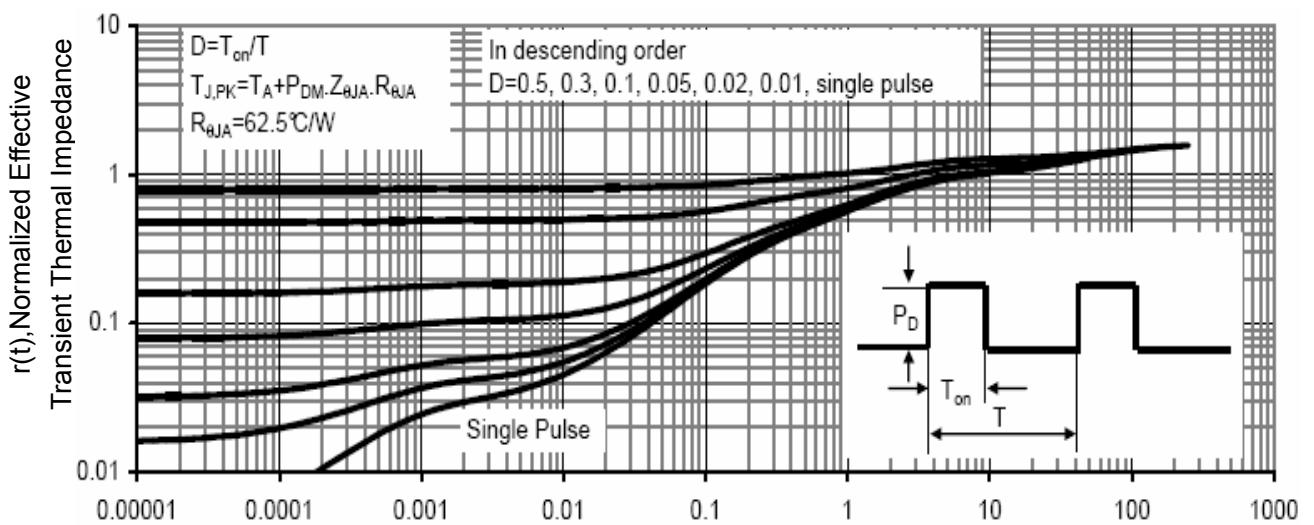
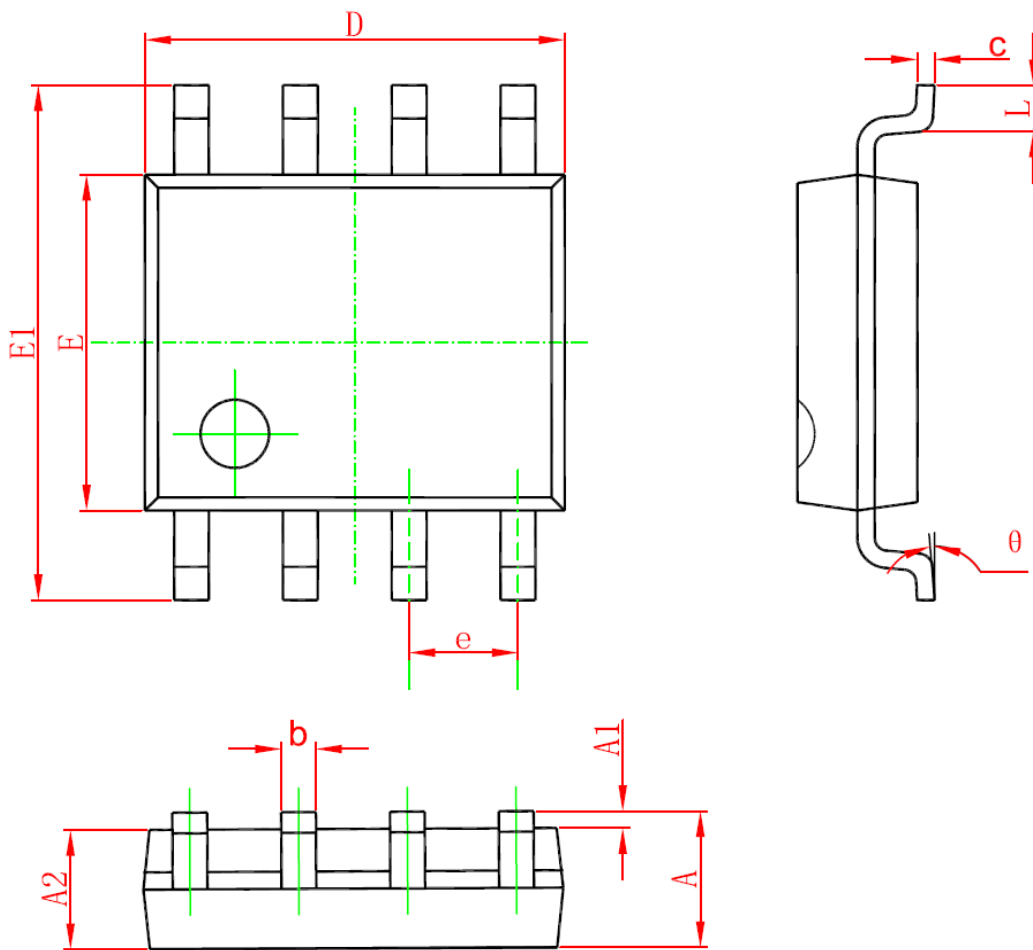


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE IN FORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°