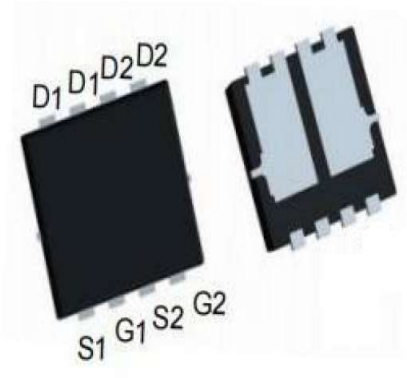
500V 5A Dual N-ch Power MOSFET

Description

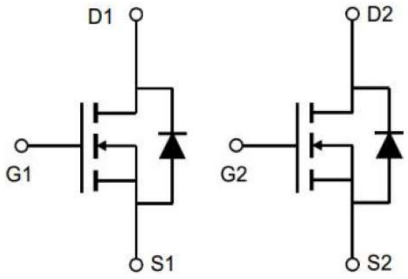
HM5DN50D is dual VDMOS family that is dramatic reduction in on-resistance and ultra-low gate charge for applications requiring high power density and high efficiency. And it is very robust and RoHS compliant.

PDFN5*6



Features

- Typ.$R_{DS(on)}$=2.6Ω@V_{GS}=10V
- 100% avalanche tested
- Pb-free，Halogen free



Applications

- SMPS
- Charger
- DC-DC

RoHS compliant

Absolute Maximum Ratings (Tc=25℃)

Parameter	Symbol	HM5DN50D	Unit
Drain-source voltage	V_{DSS}	500	V
Gate-source voltage	V_{GS}	±30	V
Continuous drain current	I_D	5	A
Pulsed drain current ①	I_{DM}	15	A
Avalanche energy, single pulse ②	E_{AS}	63	mJ
Power dissipation ①	P_D	50	W
Storage temperature	T_{stg}	-55~150	℃
Continuous diode forward current	I_S	5	A

Thermal Characteristic

Thermal resistance,junction-to-case	$R_{\theta JC}$	3	℃/W
Thermal resistance,junction-to-ambient	$R_{\theta JA}$	62.5	℃/W

Electrical Characteristics of MOSFET

				Min.	Typ.	Max.	
Drain-source break down voltage	BV_{DSS}	I_D=250uA, V_{GS}=0V	T_C=25℃	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	I_D=250uA, V_{DS}=V_{GS}	T_J=25℃	2.0	3.0	4.0	V
Drain-source leakage current	I_{DSS}	V_{DS}=500V, V_{GS}=0V	T_J=25℃	-	-	1	uA
		V_{DS}=400V, V_{GS}=0V	T_J=125℃	-	-	100	uA
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=1.5A ③	T_J=25℃	-	2.6	3.2	Ω

Dynamic Characteristics of MOSFET (T_C=25℃)

				Min.	Typ.	Max.	
Input capacitance	C_{iss}	f=1MHz, V_{DS}=25V, V_{GS}=0V		-	218	-	pF
Output capacitance	C_{oss}			-	28	-	pF
Reverse transfer capacitance	C_{rss}			-	4	-	pF
Gate to source charge	Q_{gs}	V_{DS}=480V		-	0.7	-	nC
Gate to drain charge	Q_{gd}	I_D=1A	③	-	2.7	-	nC
Total gate charge	Q_g	V_{GS}= 10V		-	4.8	-	nC

Switching Characteristics of MOSFET (T_C=25℃)

				Min.	Typ.	Max.	
Turn-off delay time	$t_{d\ off}$	V_{DD}=300V, I_D=3A, R_G=25Ω	③	-	13	-	ns

Characteristics of Body Diode (T_C=25℃)

				Min.	Typ.	Max.	
Forward voltage	V_{SD}	I_S=3A, V_{GS}=0V, Tj=25℃	③	-	-	1.4	V
Reverse recovery time	t_{rr}	If=3A, Tj=25℃	③	-	62	-	ns
Recovery charge	Q_{rr}	di/dt=100A/us		-	0.28	-	uC

Note:

1. ID & PD base on maximum allowable junction temperature, test at Tc=25℃.
2. Starting Tj=25℃, VDD =50V, L=30mH, RG =25Ω, IAS=3.0A
3. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%

TYPICAL CHARACTERISTICS

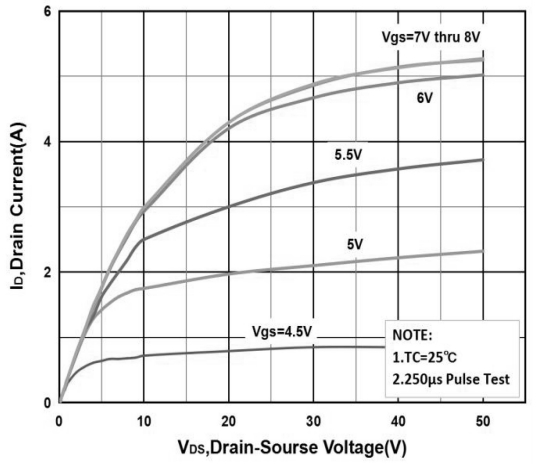


Figure 1.Typical Output Characteristics, Tc=25℃

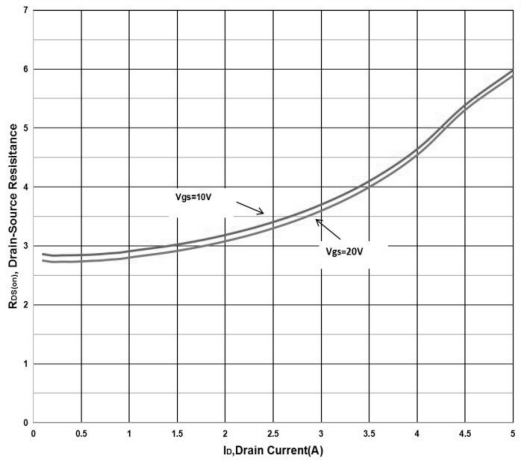


Figure 2. On-Resistance Vs.Drain Current and Gate Voltage

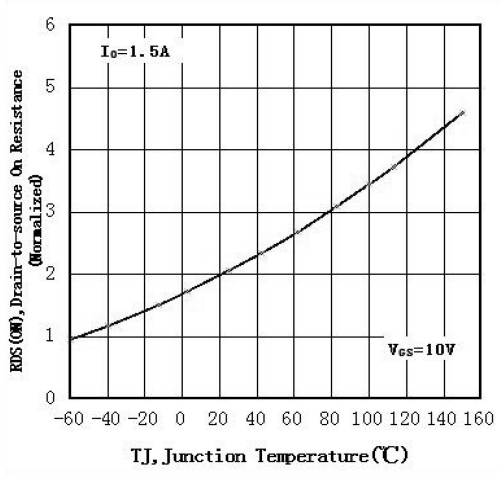


Figure 3. Normalized On-Resistance Vs.Temperature

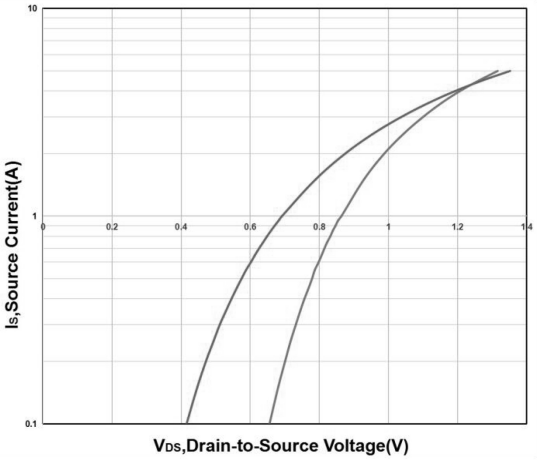


Figure 4. Typical Source-Drain Diode Forward Voltage

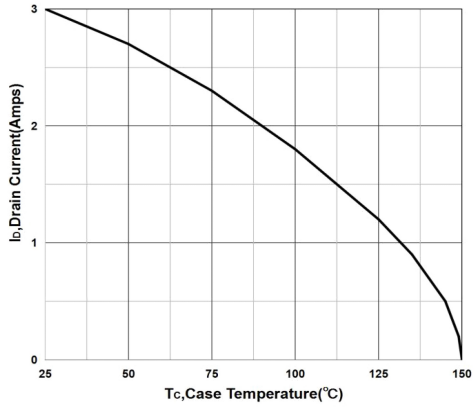


Figure 5. Maximum Drain Current Vs.Case Temperature

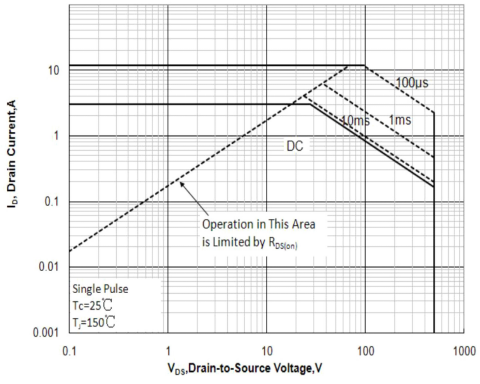
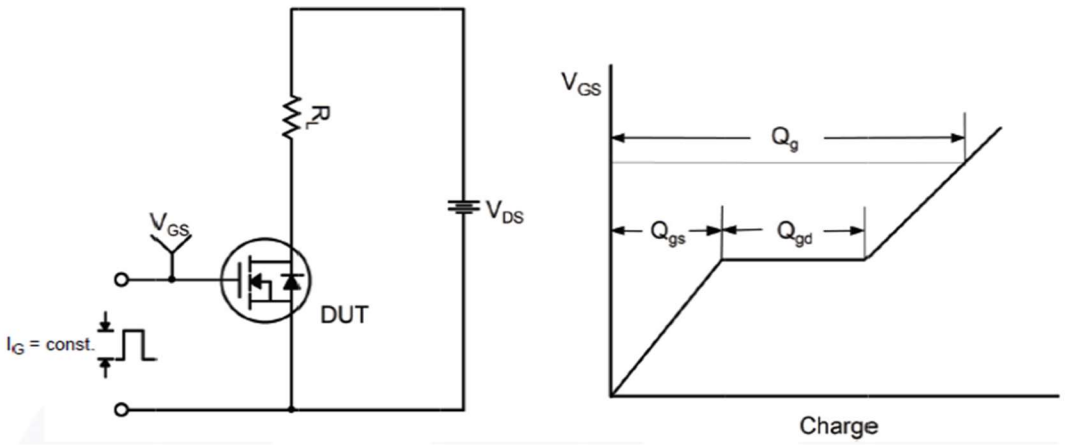
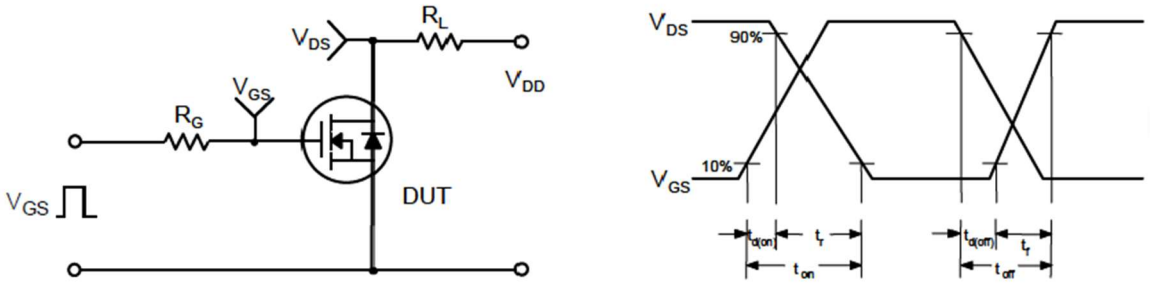


Figure 6. Maximum Safe Operating Area

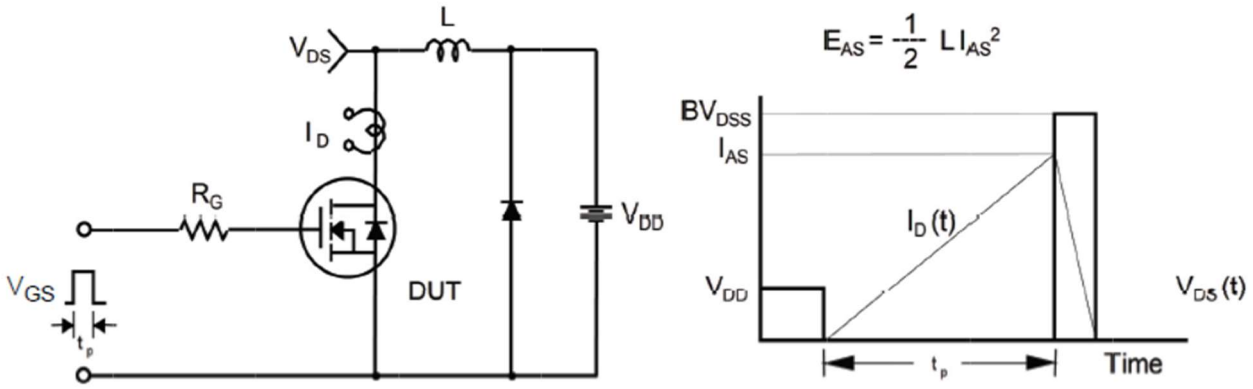
Gate Charge Test Circuit &Waveform



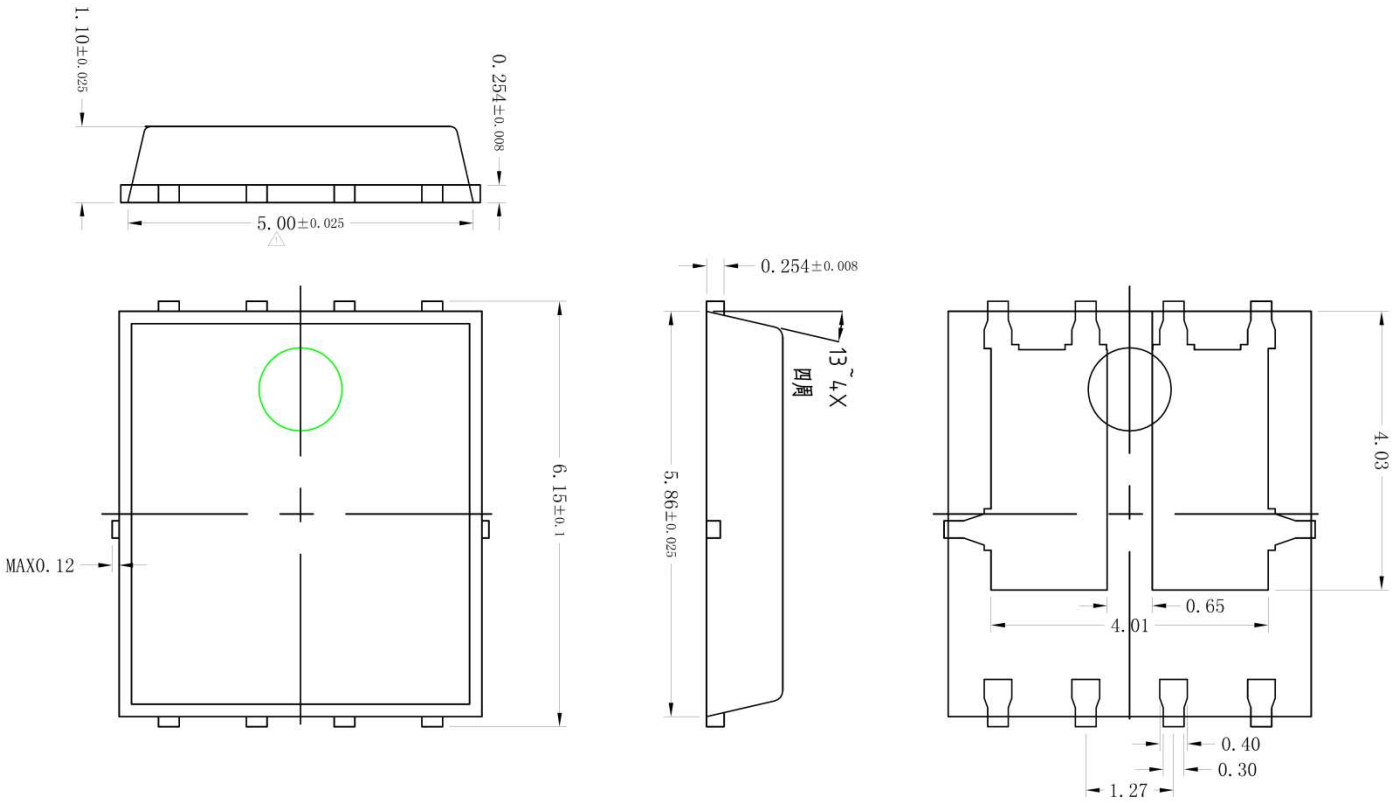
Switching Test Circuit &Waveforms



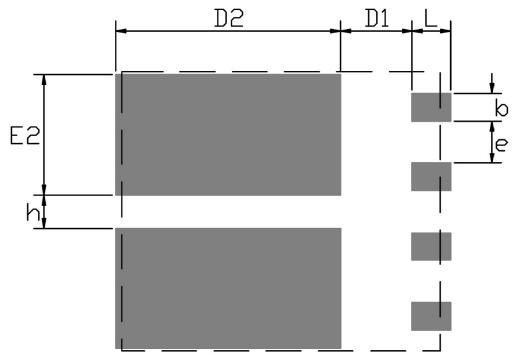
Unclamped Inductive Switching Test Circuit &Waveforms



Mechanical Dimensions for PDFN5*6



PAD Layout for PDFN5*6



SYMBOL	MILLIMETER
	NOM
b	0.5
e	0.77
D1	1.3
D2	4.1
E2	2.2
L	0.7
h	0.6