

Description

The HM5N15Q uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

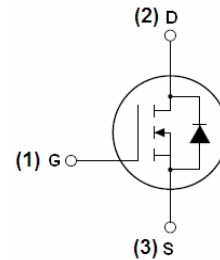
- $V_{DS} = 150V, I_D = 5A$
 $R_{DS(ON)} < 300m\Omega @ V_{GS} = 10V$ (Typ: 70m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

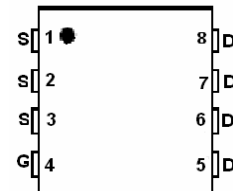
- Boost converters
- LED backlighting
- Uninterruptible power supply

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM5N15Q	HM5N15Q	DFN3X3-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	5	A
$I_D(100^\circ C)$	Drain Current-Continuous($T_C = 100^\circ C$)	3.5	A
I_{DM}	Pulsed Drain Current	15	A
P_D	Maximum Power Dissipation	75	W
	Derating factor	0.5	W/ $^\circ C$
E_{AS}	Single pulse avalanche energy ^(Note 5)	200	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ^(Note 2)	2.0	$^\circ C/W$
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

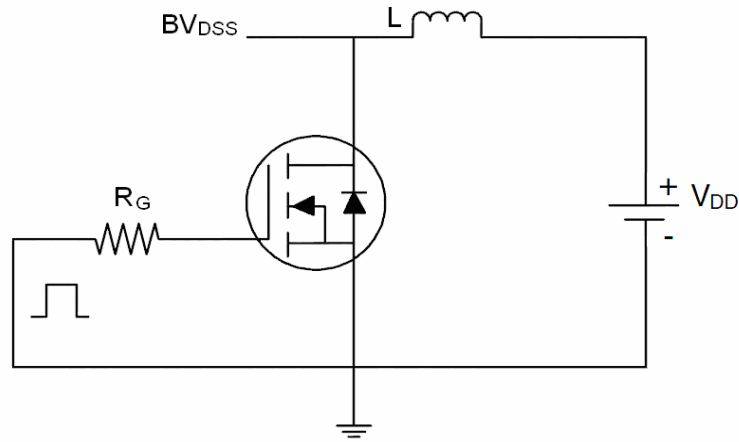
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	150	165	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=150V, V_{GS}=0V$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.5	2	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=10A$	-	260	300	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5V, I_D=10A$	-	20	-	S
Dynamic Characteristics (Note 4)						
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	2000	-	PF
C_{oss}	Output Capacitance		-	290	-	PF
C_{rss}	Reverse Transfer Capacitance		-	180	-	PF
Switching Characteristics (Note 4)						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=75V, R_L=5\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	10.5	-	nS
t_r	Turn-on Rise Time		-	5.5	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	14.5	-	nS
t_f	Turn-Off Fall Time		-	3	-	nS
Q_g	Total Gate Charge	$V_{DS}=75V, I_D=10A,$ $V_{GS}=10V$	-	17	-	nC
Q_{gs}	Gate-Source Charge		-	4	-	nC
Q_{gd}	Gate-Drain Charge		-	4.4	-	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage (Note 3)	$V_{GS}=0V, I_S=8A$	-	-	1.2	V
I_S	Diode Forward Current (Note 2)	-	-	-	5	A
t_{rr}	Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_F = 10A$ $di/dt = 100A/\mu s$ (Note 3)	-	32	-	nS
Q_{rr}	Reverse Recovery Charge		-	53	-	nC
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

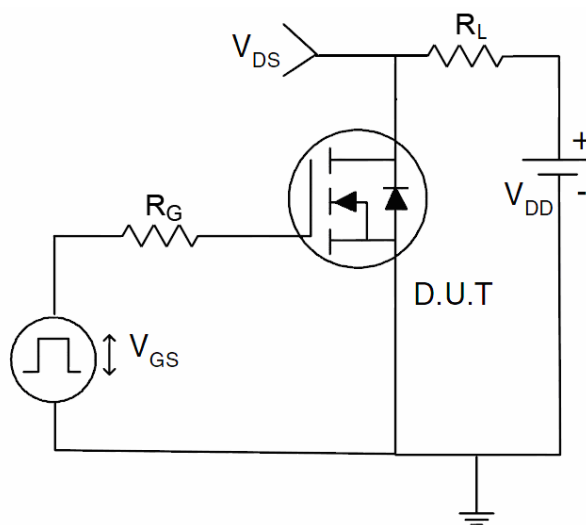
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

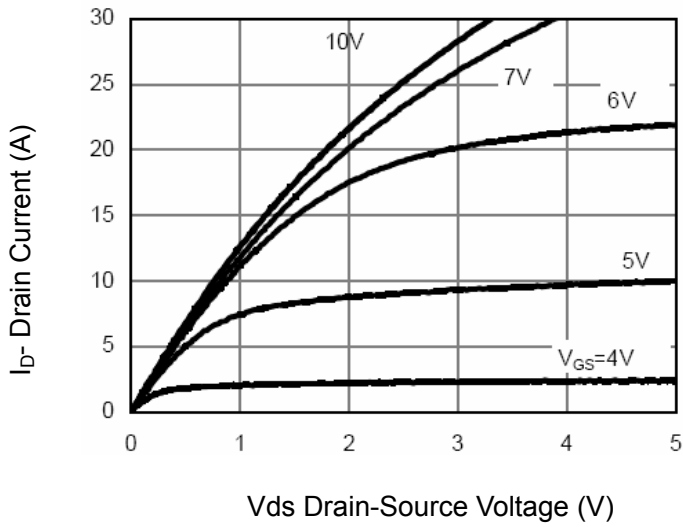


Figure 1 Output Characteristics

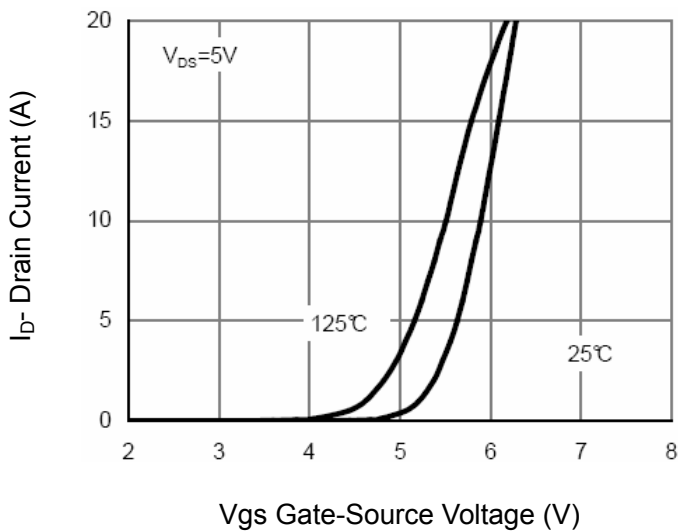


Figure 2 Transfer Characteristics

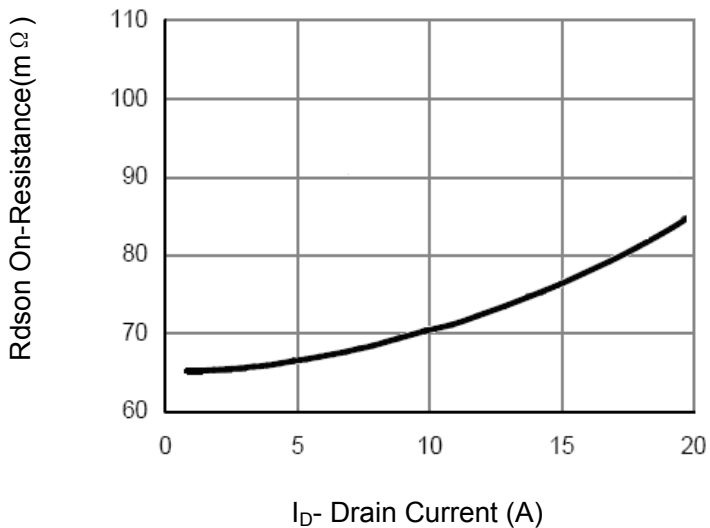


Figure 3 Rdson- Drain Current

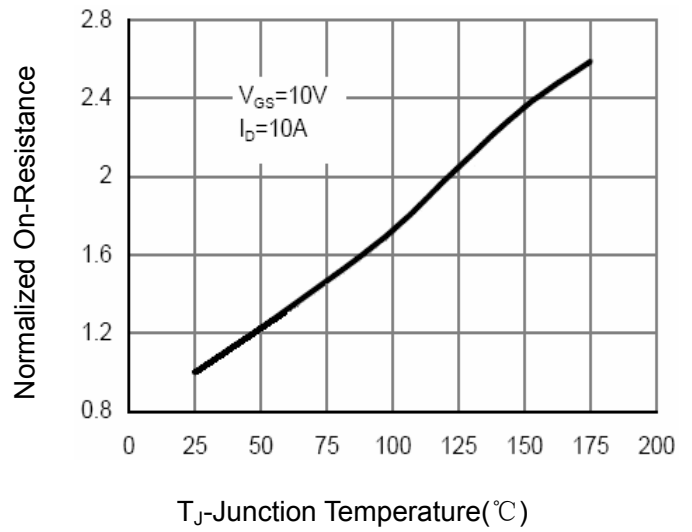


Figure 4 Rdson-Junction Temperature

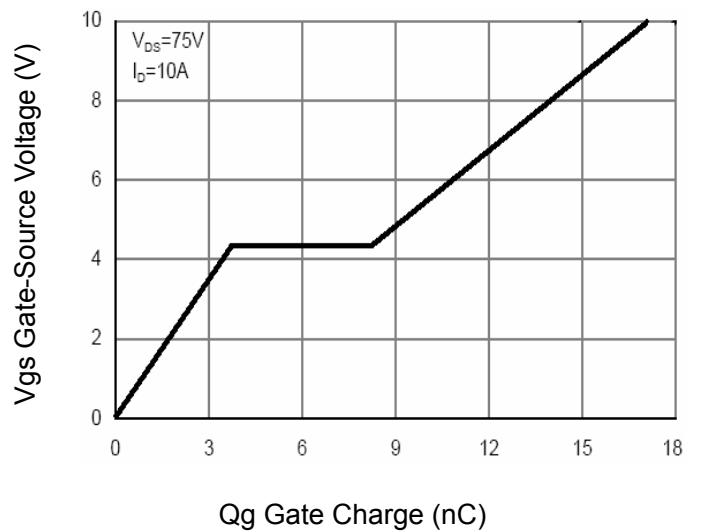


Figure 5 Gate Charge

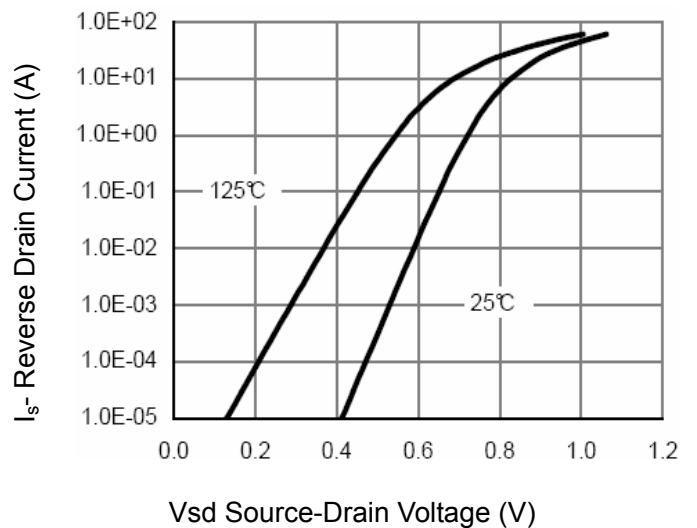


Figure 6 Source- Drain Diode Forward

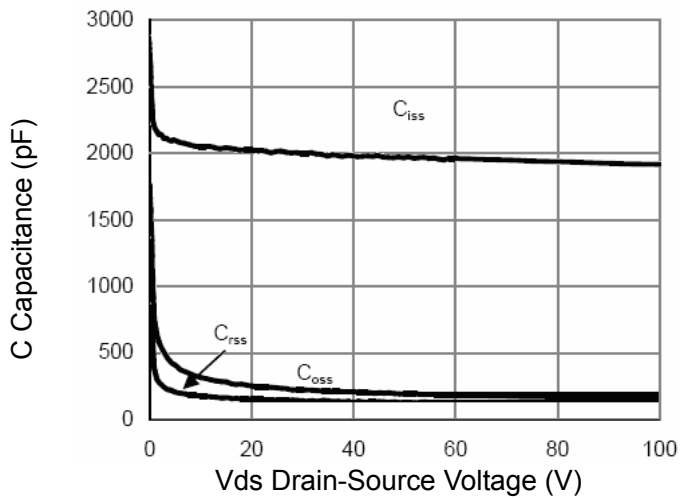


Figure 7 Capacitance vs Vds

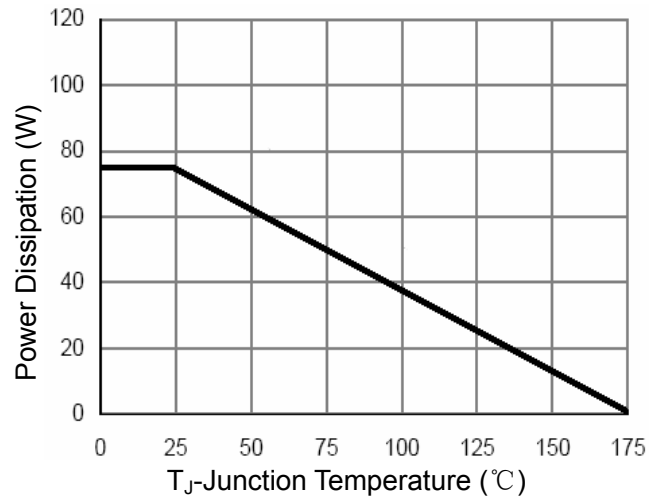


Figure 9 Power De-rating

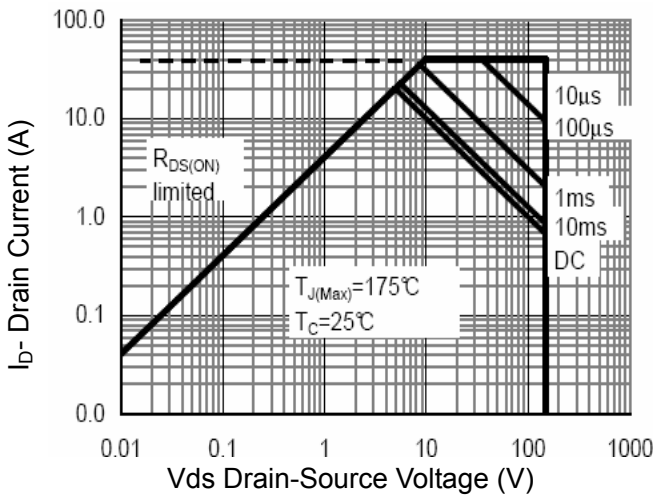


Figure 8 Safe Operation Area

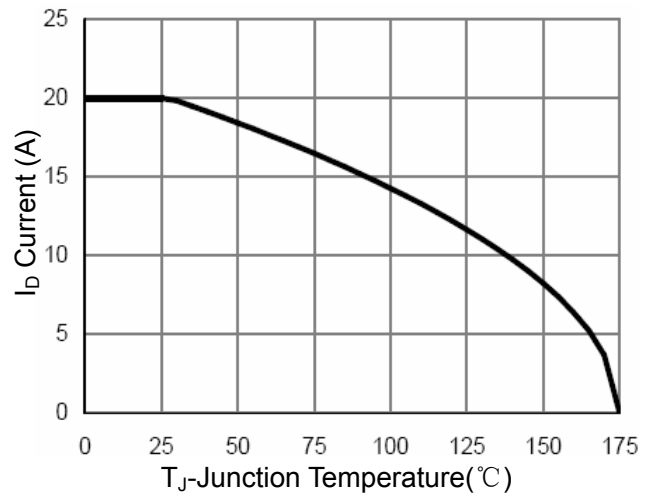


Figure 10 ID Current- Junction Temperature

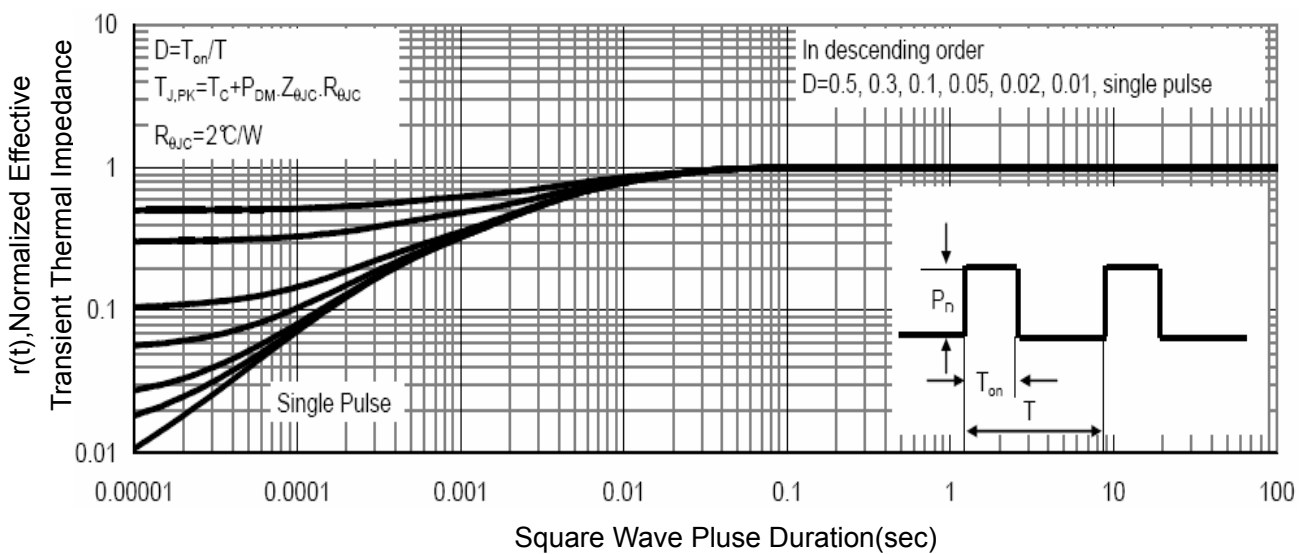
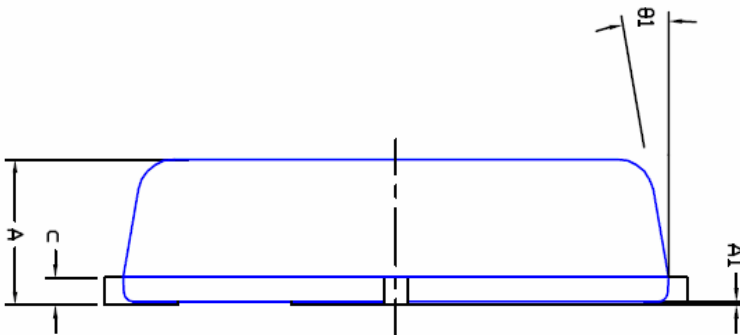
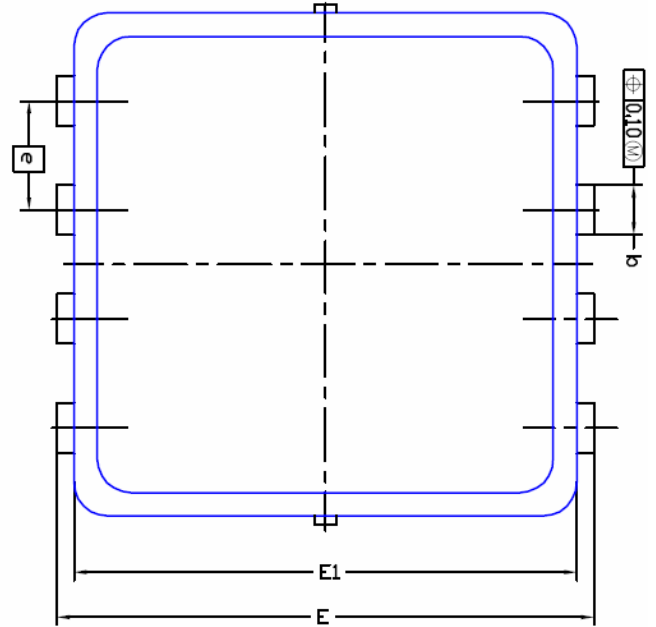
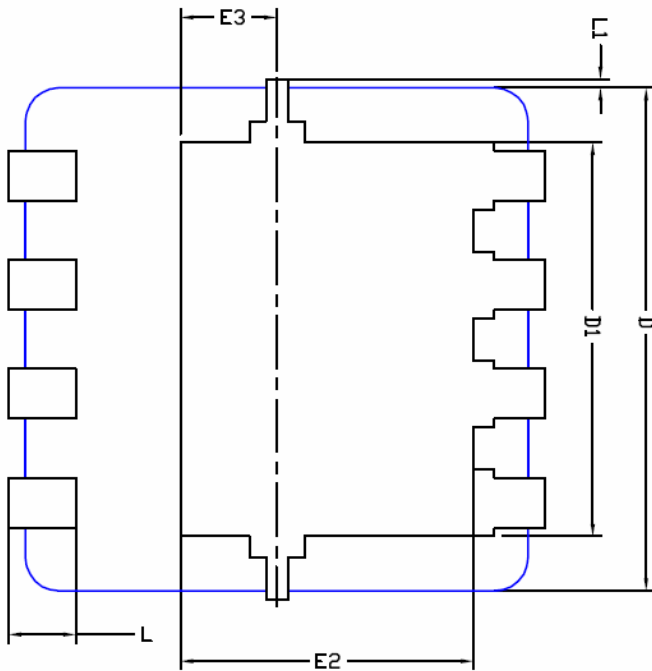


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3X3 EP Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ_1	0°	10°	12°	0°	10°	12°