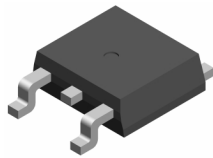# HM9N50K/HM9N50I

500V N-Channel MOSFET

General Description

This Power MOSFET is produced using SL semi's advanced planar stripe DMOS technology.
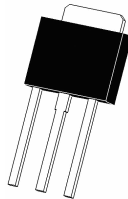This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency sw itched mode power supplies, active power factor correction based on half bridge topology.
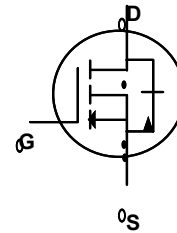
Features

- 9A, 500V, $R_{DS(on)}$ = 0.95Ω @V_{GS} = 10 V
- Low gate charge (typical 16nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

TO-252   **TO-251**

Absolute Maximum Ratings T_C = 25°Cunless otherwise noted

Symbol	Parameter		HM9N50K	HM9N50I	Units
V_{DSS}	Drain-Source Voltage		500		V
I_D	Drain Current - Continuous (T_C = 25°C)		9	9*	A
	- Continuous (T_C = 100°C)		6.3	6.3 *	A
I_{DM}	Drain Current - Pulsed	(Note 1)	27	27 *	A
V_{GSS}	Gate-Source Voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	210		mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	10.0		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns
P_D	Power Dissipation (T_C = 25°C)		100	33	W
	- Derate above 25°C		0.8	0.26	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		°C

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	HM9N50K	HM9N50I	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.25	3.79	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.6	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 480 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 2.25 A	--	0.695	0.95	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	560	--	pF
C_{oss}	Output Capacitance		--	55	--	pF
C_{rss}	Reverse Transfer Capacitance		--	7	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 9A, R_G = 25 Ω	--	10	--	ns
t_r	Turn-On Rise Time		--	40	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	40	--	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	50	--	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 9A, V_{GS} = 10 V	--	16	-	nC
Q_{gs}	Gate-Source Charge		--	2.5	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	6.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	9	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	27	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 9 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 9 A, dI_F / dt = 100 A/μs (Note 4)	--	300	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.0	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 19 mH, I_{AS} = 9 A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 9 A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature
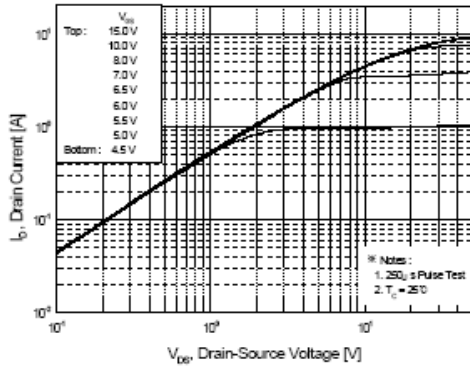
Typical Characteristics

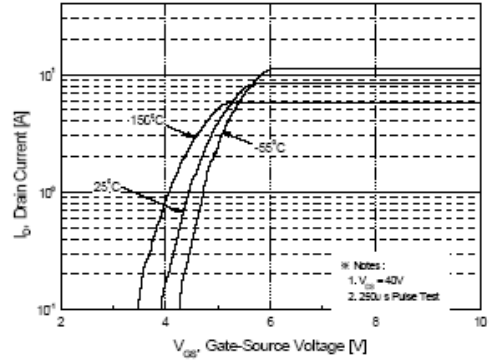Figure 1. On-Region Characteristics

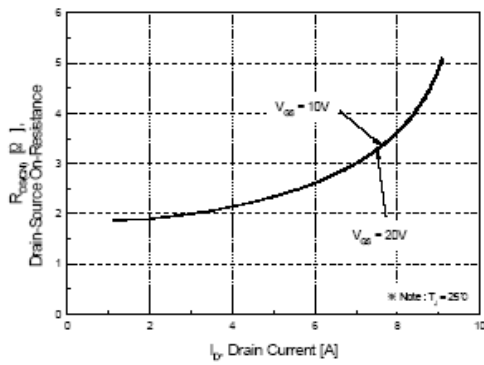Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs
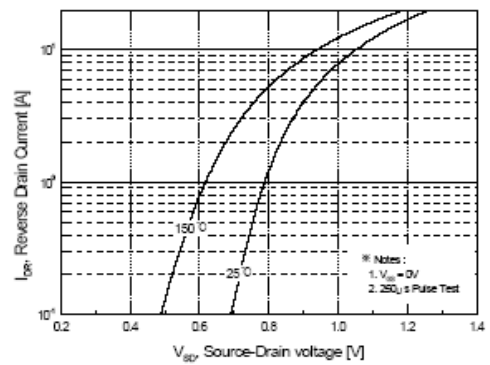Drain Current and Gate Voltage

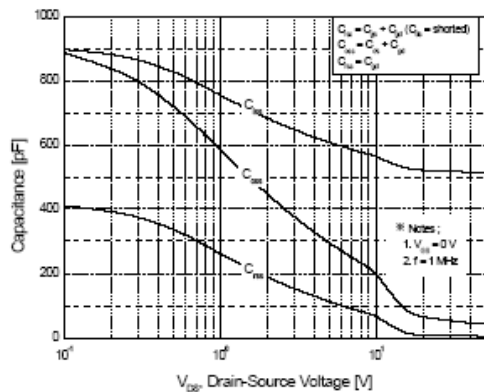Figure 4. Body Diode Forward Voltage
Variation with Source Current

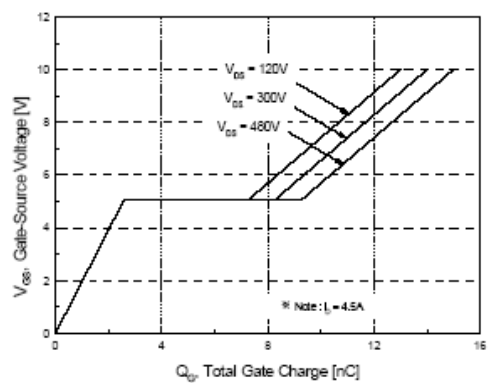Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics
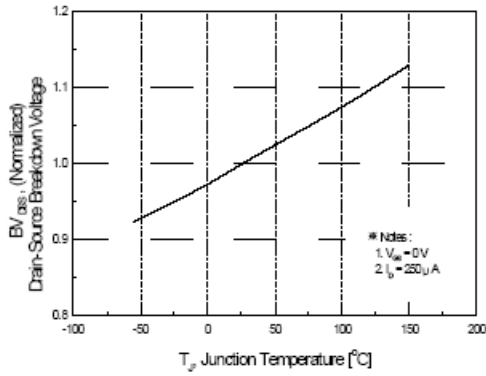
Typical Characteristics (Continued)

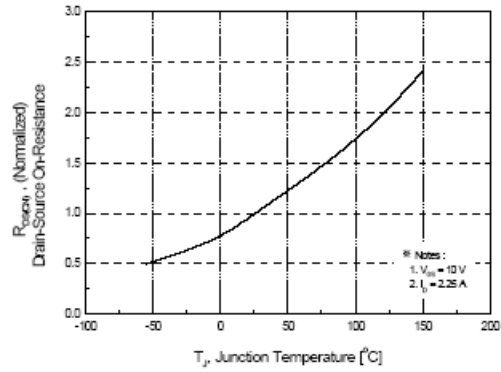

Figure 7. Breakdown Voltage Variation
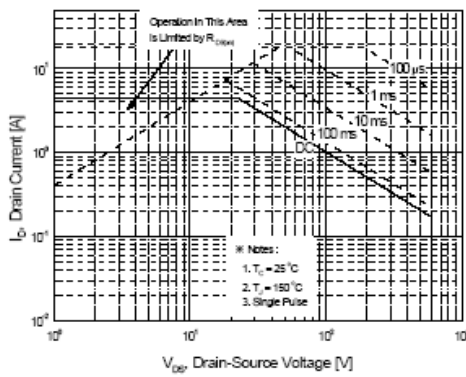vs Temperature

Figure 8. On-Resistance Variation
vs Temperature

Figure 9-1. Maximum Safe Operating Area
for HM9N50K
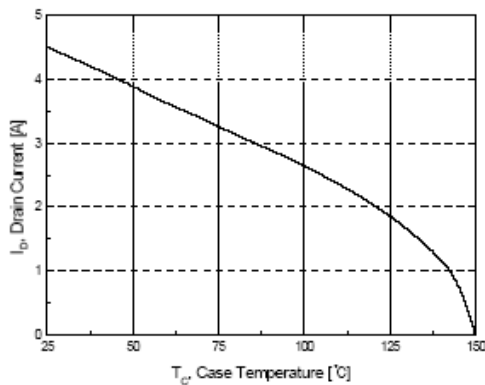

Figure 9-2. Maximum Safe Operating Area
for HM9N50I

Figure 10. Maximum Drain Current
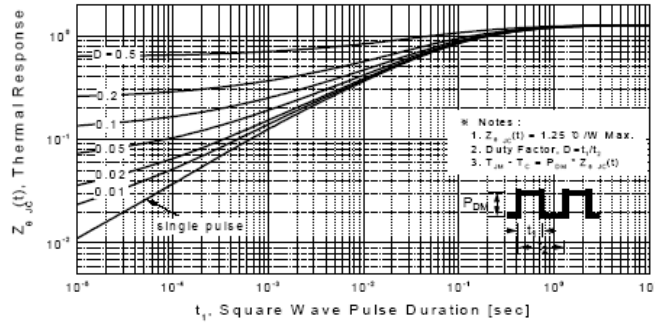vs Case Temperature

Typical Characteristics (Continued)

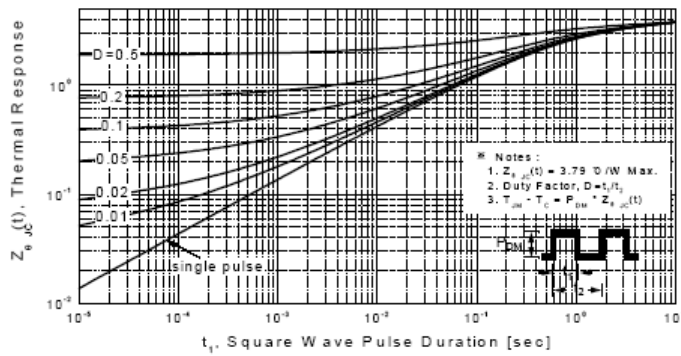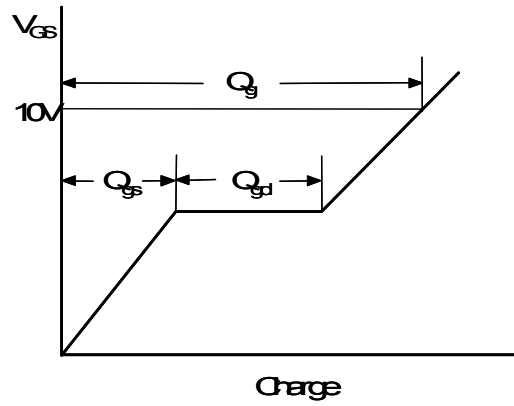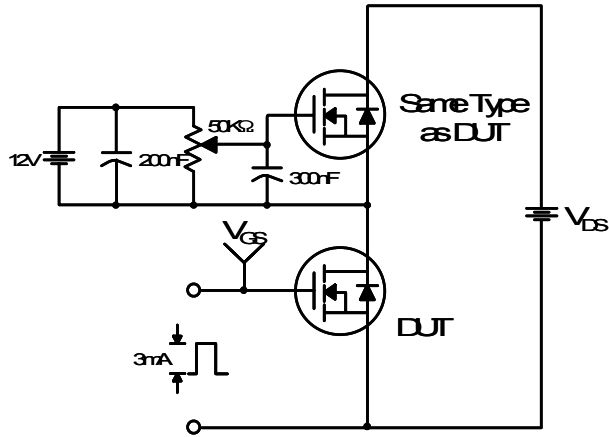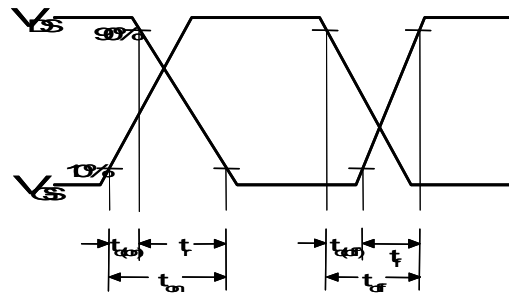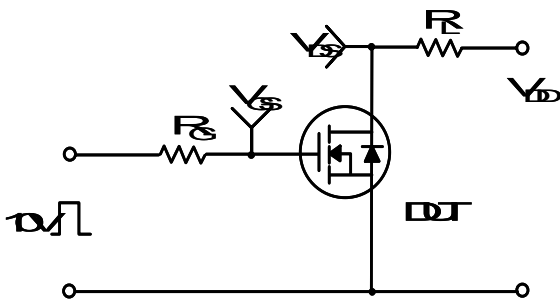**Figure 11-1. Transient Thermal Response Curve for HM9N50K**

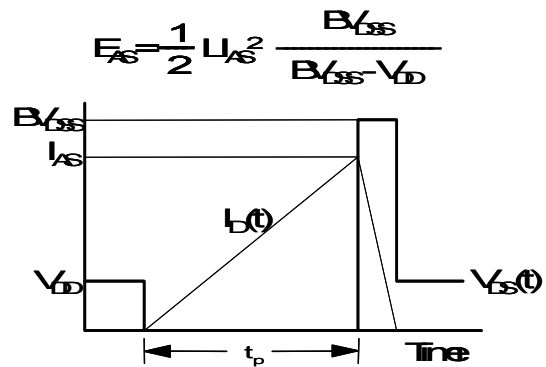**Figure 11-2. Transient Thermal Response Curve for HM9N50I**
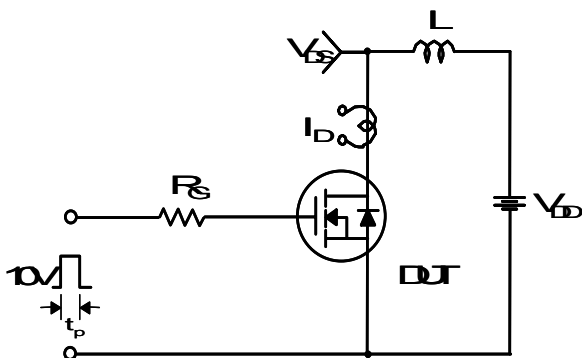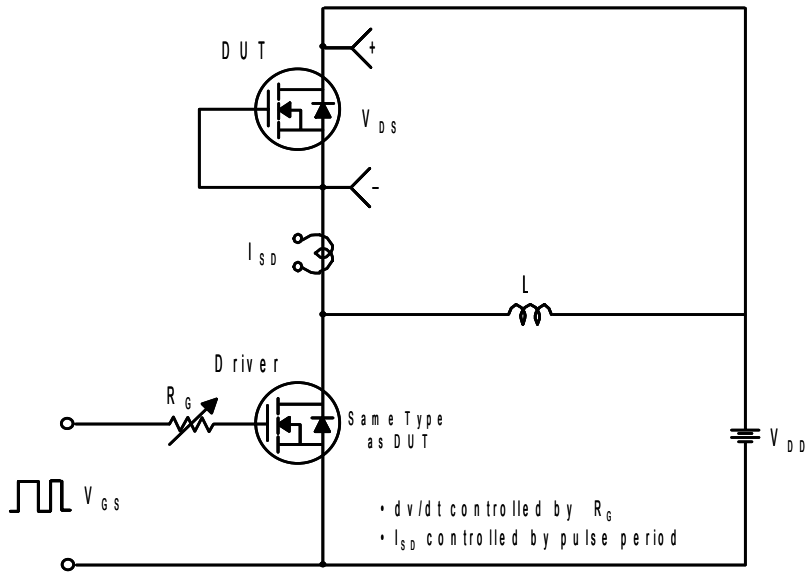
Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO-252-2L PACKAGE OUTLINE DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	

虹美功率半导体

TO-251 PACKAGE OUTLINE DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	1.050	1.350	0.042	0.054
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311