

HMS11N65K
650V N-Channel Super Junction MOSFET

Features

- Very Low FOM ($R_{DS(on)} \times Q_g$)
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche Tested
- Built-in ESD Diode

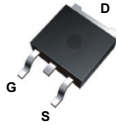
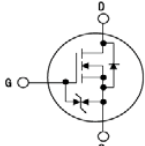
Application

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- TV power & LED Lighting Power
- AC to DC Converters
- Telecom

Key Parameters

Parameter	Value	Unit
$BV_{DSS} @T_{j,max}$	700	V
I_D	11	A
$R_{DS(on), typ}$	0.27	Ω
Q_g, Typ	22.6	nC

Package & Internal Circuit

D-PAK	SYMBOL
	

Absolute Maximum Ratings $T_C=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous ($T_C = 25^{\circ}C$)	11	A
	Drain Current - Continuous ($T_C = 100^{\circ}C$)	7.7	A
$I_{DM}^{1)}$	Drain Current - Pulsed	33	A
$E_{AS}^{2)}$	Single Pulsed Avalanche Energy	133	mJ
I_{AR}	Avalanche Current	1.75	A
dv/dt	MOSFET dv/dt ruggedness, $V_{DS}=0 \dots 400V$	50	V/ns
dv/dt	Reverse diode dv/dt, $V_{DS}=0 \dots 400V, I_{DS} \leq I_D$	15	V/ns
P_D	Power Dissipation ($T_C = 25^{\circ}C$)	91	W
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	2000	V
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^{\circ}C$

Thermal Resistance Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.37	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient , Max.	62.5	$^{\circ}C/W$

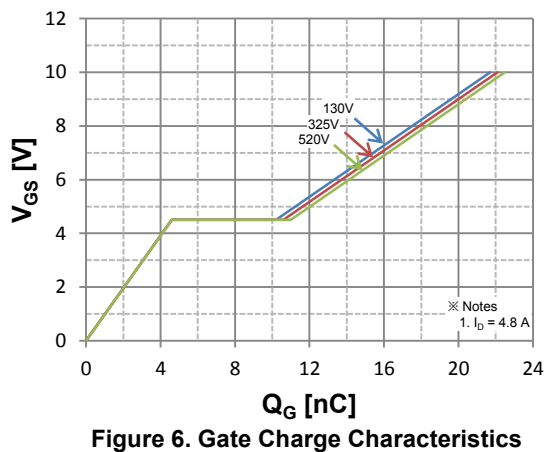
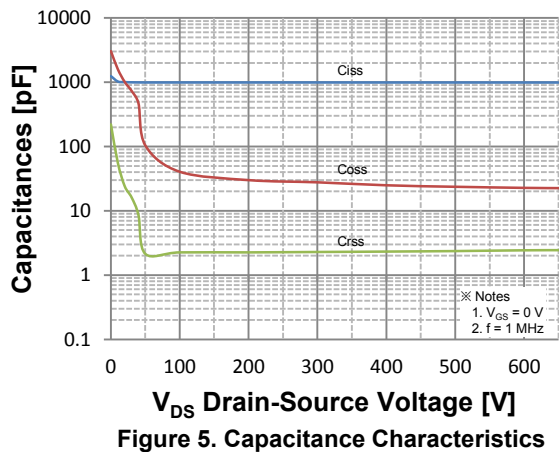
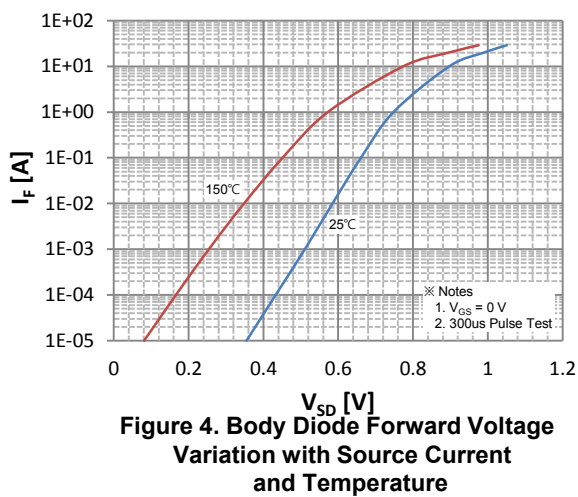
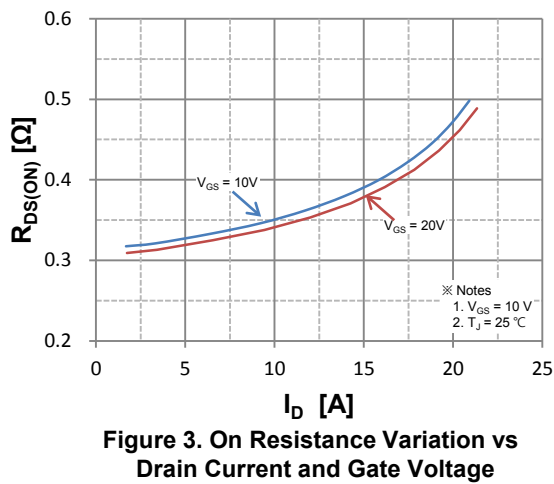
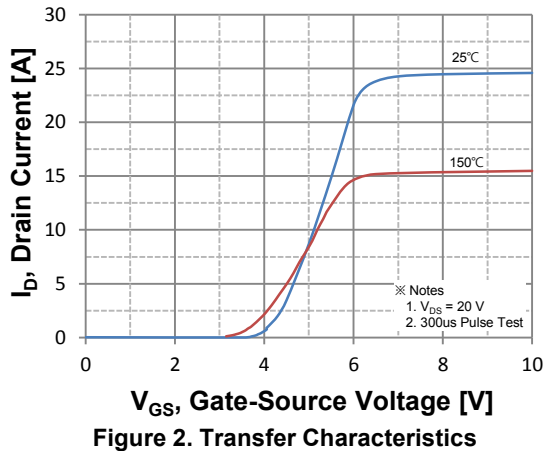
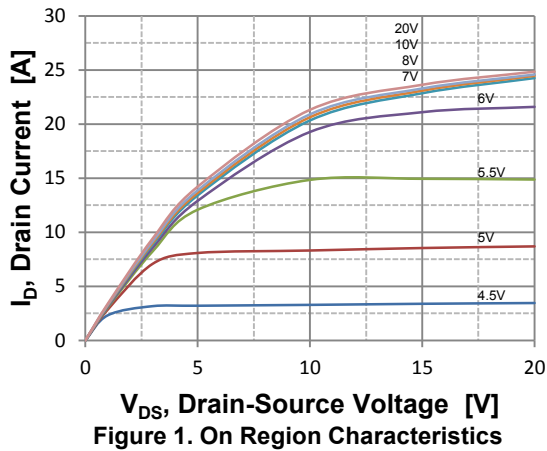
Electrical Characteristics $T_J=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
On Characteristics						
V _{GS}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 370 μA	2.8	-	3.8	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 3.4 A	-	0.27	0.30	Ω
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1mA	650	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0	-	-	1	μA
		V _{DS} = 650 V, T _C = 150°C	-	-	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	±1	μA
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1.0 MHz	-	990	-	pF
C _{oss}	Output Capacitance		-	25	-	pF
C _{rss}	Reverse Transfer Capacitance		-	2.5	-	pF
Switching Characteristics						
t _{d(on)}	Turn-On Time	V _{DS} = 325 V, I _D = 4.8 A, R _G = 25 Ω (Note 3,4)	-	28	-	ns
t _r	Turn-On Rise Time		-	20	-	ns
t _{d(off)}	Turn-Off Delay Time		-	114	-	ns
t _f	Turn-Off Fall Time		-	17	-	ns
Q _{g(}	Total Gate Charge	V _{DS} = 520 V, I _D = 4.8 A, V _{GS} = 10 V (Note 3,4)	-	22.6	-	nC
Q _{gs}	Gate-Source Charge		-	4.6	-	nC
Q _{gd}	Gate-Drain Charge		-	6.4	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		-	-	11	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	33	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 4.8 A	-	-	1.3	V
t _{rr}	Reverse Recovery Time	V _R = 400 V, I _F = 4.8 A di _F /dt = 100 A/μs	-	250	-	ns
Q _{rr}	Reverse Recovery Charge		-	2.6	-	μC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{AS}=1.75\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
3. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
4. Essentially Independent of Operating Temperature

Typical Characteristics



Typical Characteristics (continued)

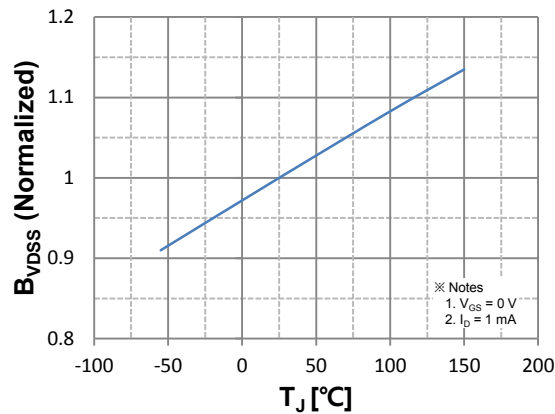


Figure 7. Breakdown Voltage Variation vs. Temperature

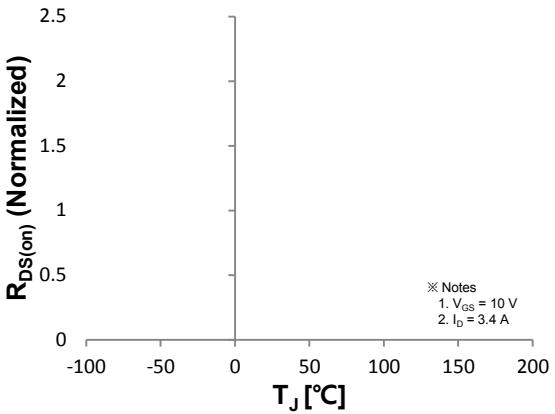


Figure 8. On-Resistance Variation vs. Temperature

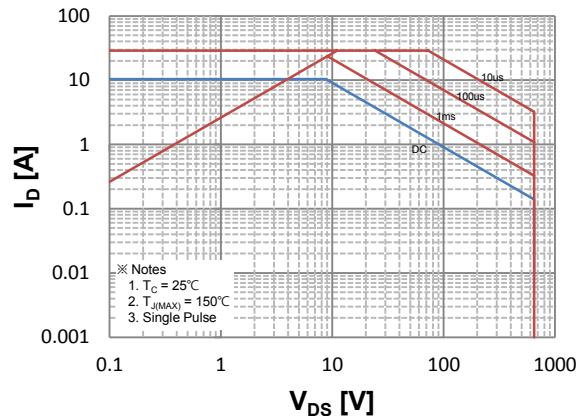


Figure 9. Maximum Safe Operating Area

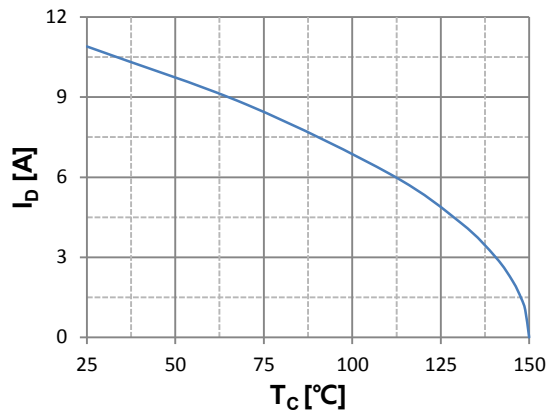


Figure 10. Maximum Drain Current vs. Case Temperature

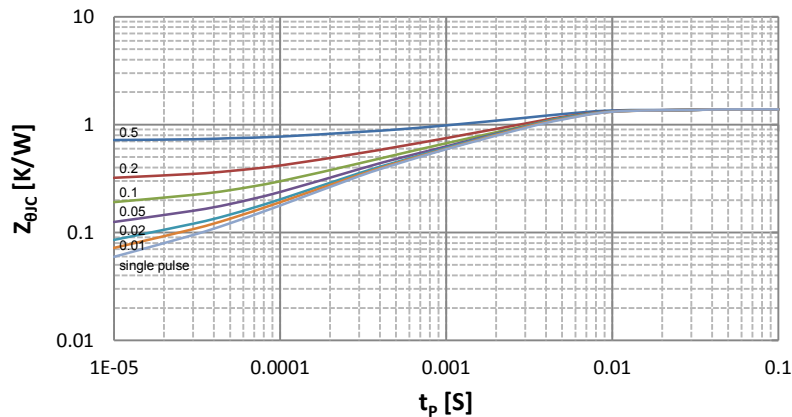


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

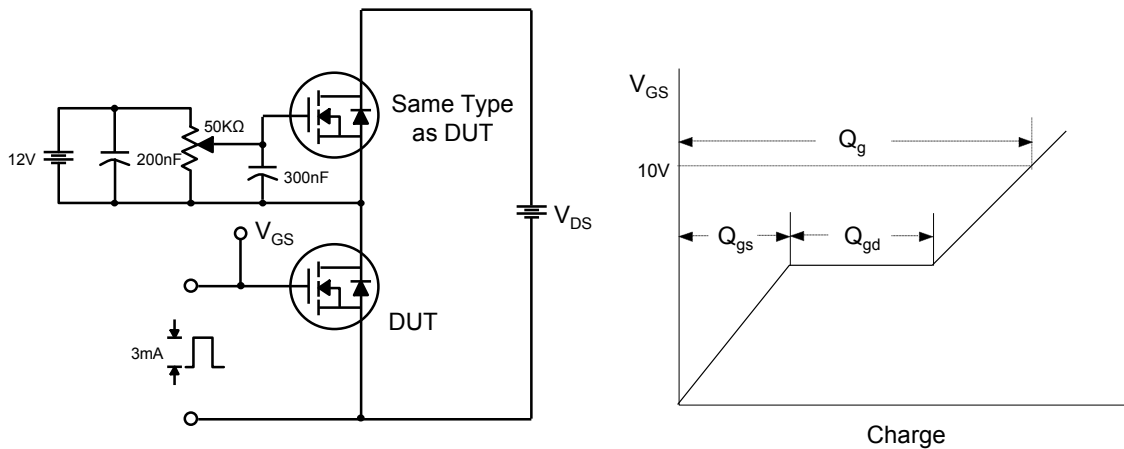


Fig 13. Resistive Switching Test Circuit & Waveforms

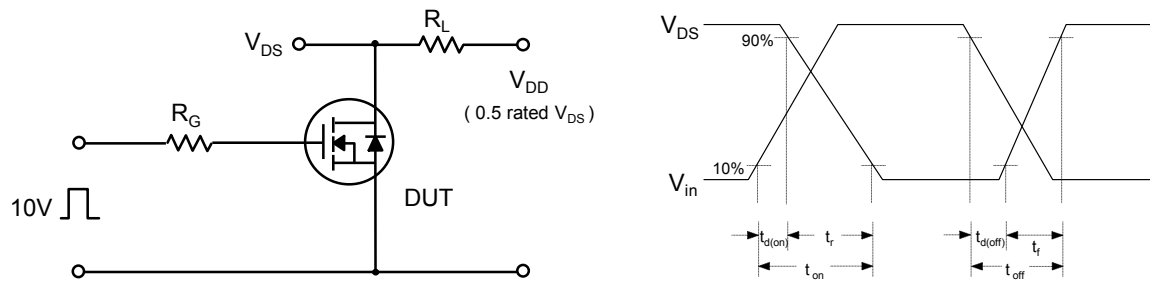


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

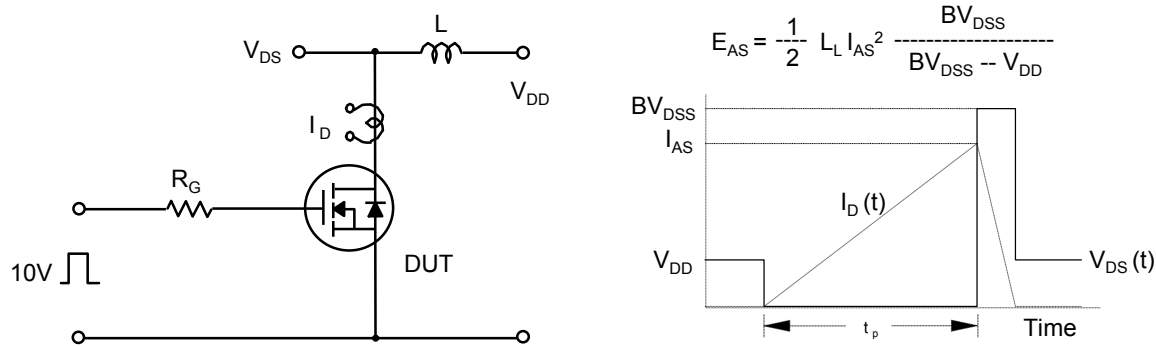
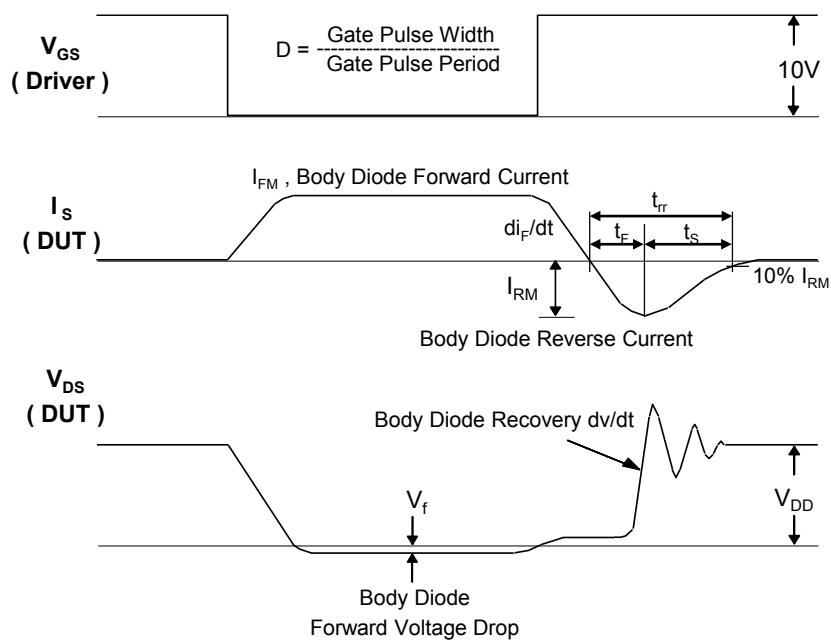
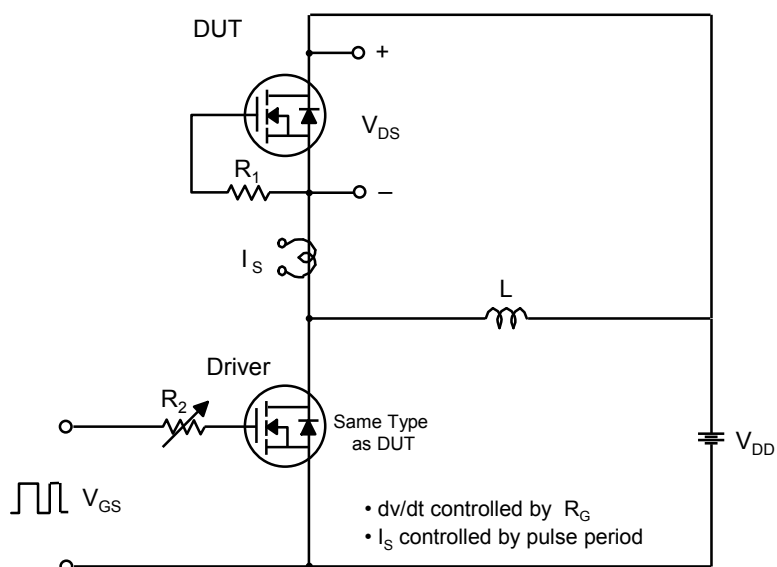


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D-PAK
(TO-252A)

